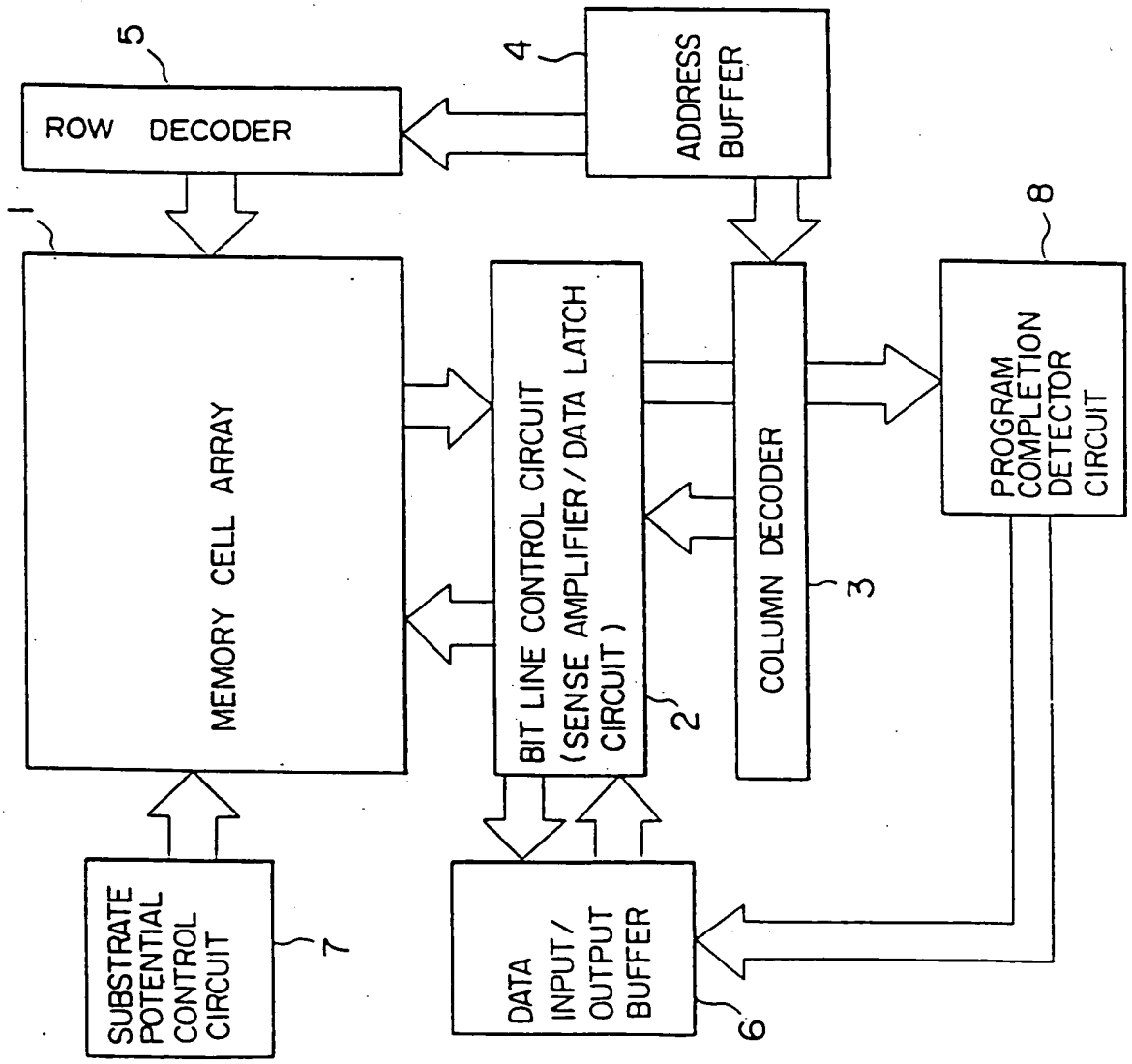

5
ROW DECODER
4
ADDRESS BUFFER
1
MEMORY CELL ARRAY
BIT LINE CONTROL CIRCUIT (SENSE AMPLIFIER / DATA LATCH CIRCUIT)
2
COLUMN DECODER
3
8
PROGRAM COMPLETION DETECTOR CIRCUIT
SUBSTRATE POTENTIAL CONTROL CIRCUIT
7
DATA INPUT / OUTPUT BUFFER
6

FIG. 1

FIG. 2(a)

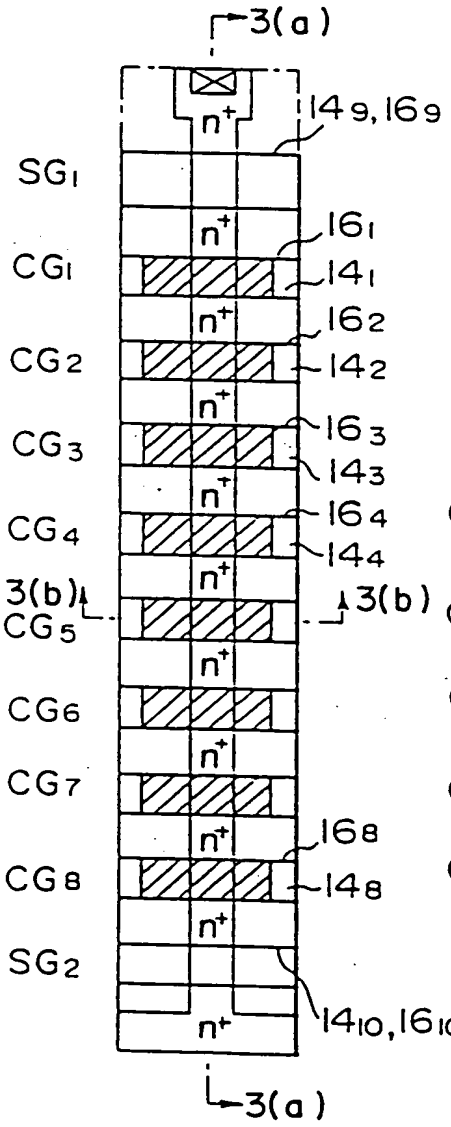

3(a)
n+
149, 169
SG1
161
CG1
141
162
CG2
142
163
CG3
143
164
CG4
144
3(b)
CG5
3(b)
CG6
CG7
168
CG8
148
SG2
1410, 1610
3(a)

FIG. 2(b)

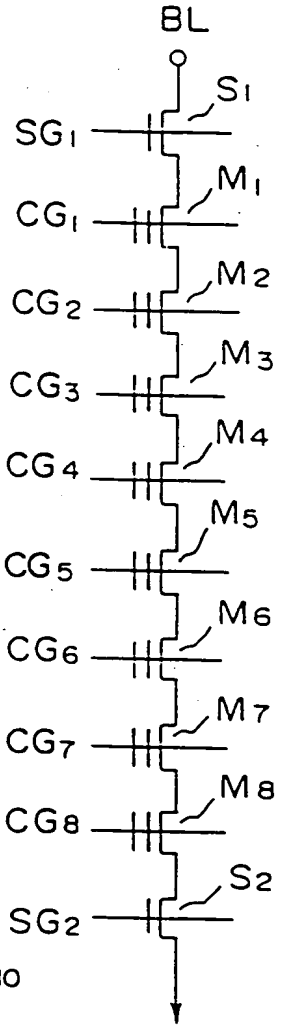

BL
S1
SG1
M1
CG1
M2
CG2
M3
CG3
M4
CG4
M5
CG5
M6
CG6
M7
CG7
M8
CG8
S2
SG2

FIG. 3(a)

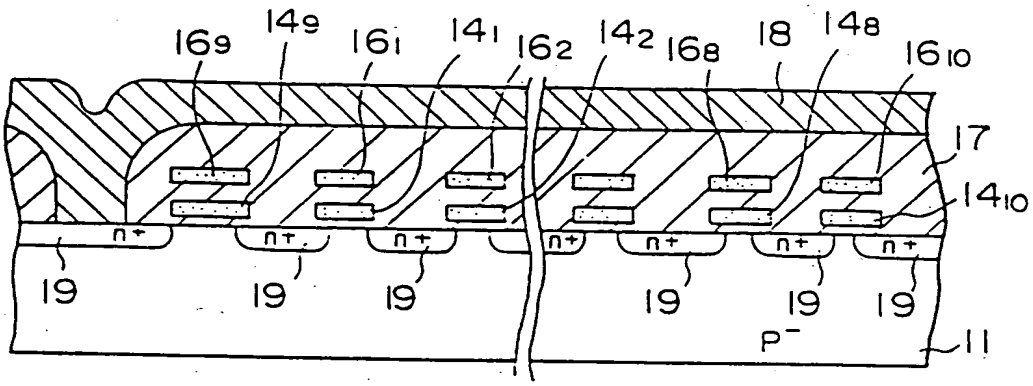
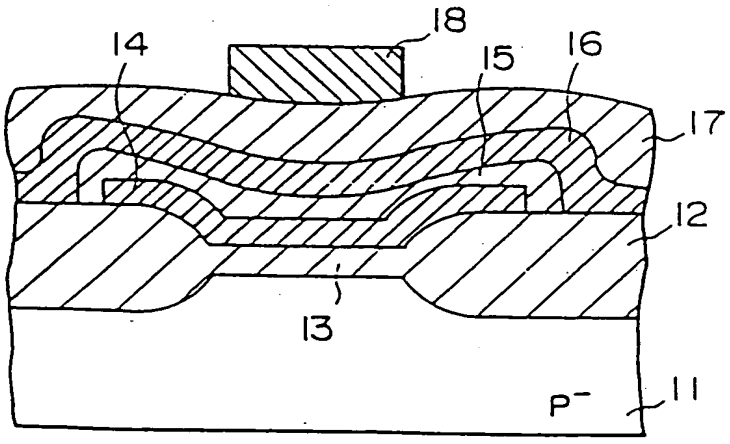

16 9
14 9
16 1
14 1
16 2
14 2
16 8
18
14 8
16 10
17
14 10
n+
19
P-
11

FIG. 3(b)


18
14
15
16
17
12
13
P-
11

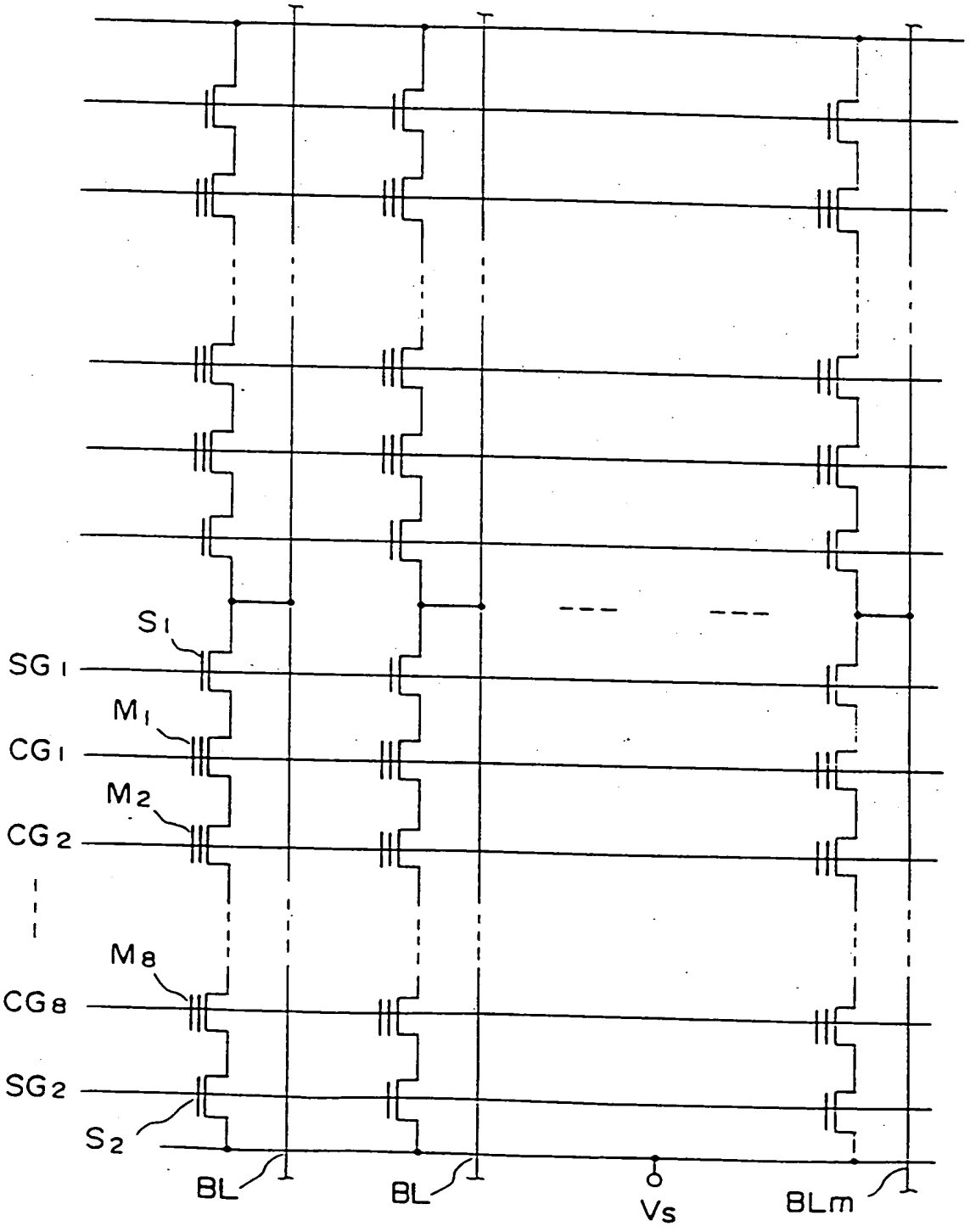


FIG. 4

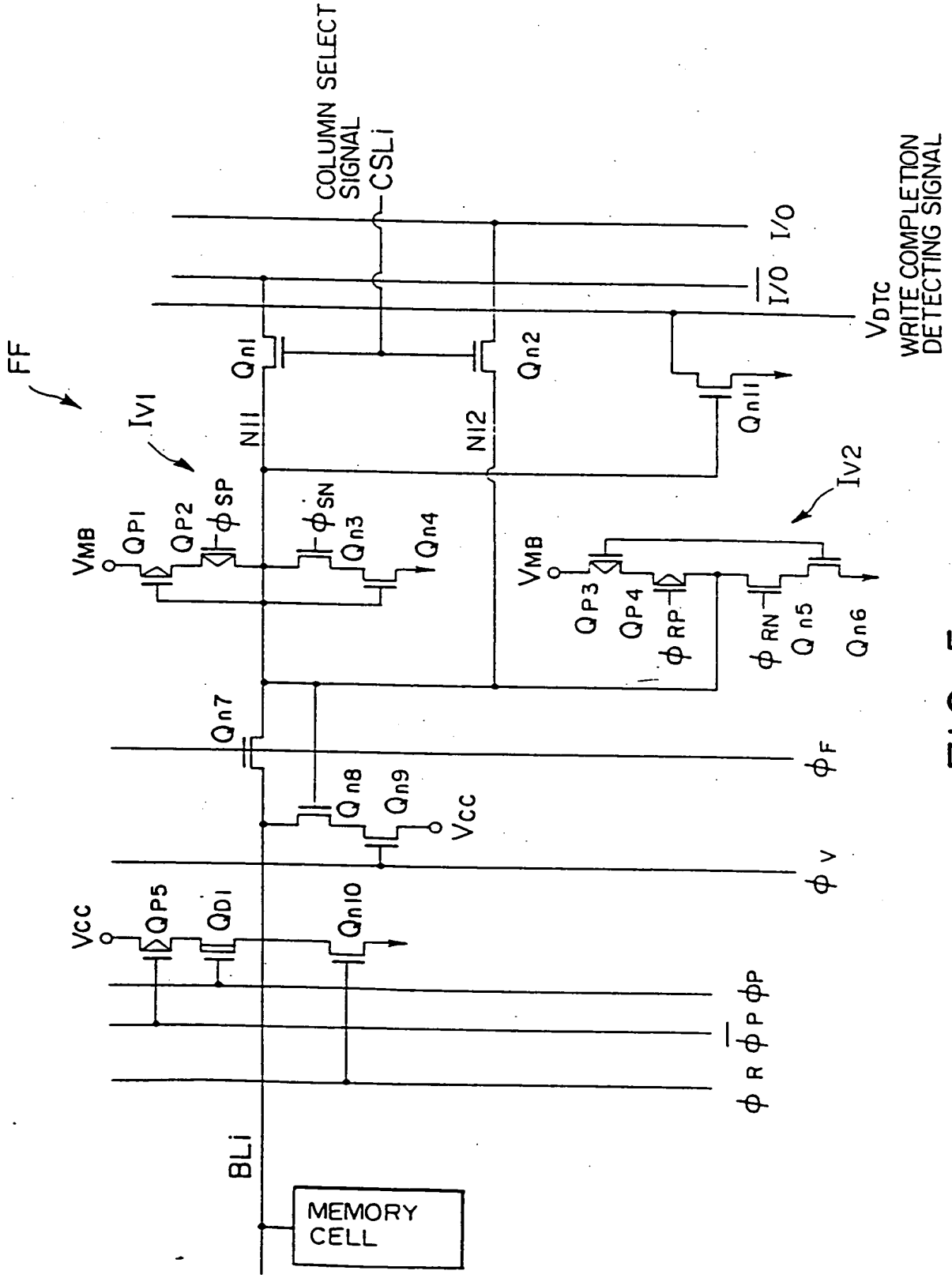

COLUMN SELECT SIGNAL CSLi
I/O
I/O
VDTC
WRITE COMPLETION DETECTING SIGNAL
FF
IV1
IV2
Qn1
Qn2
Qn11
N11
N12
VMB
QP1
QP2
φSP
φSN
Qn3
Qn4
QP3
QP4
φRP
φRN
Qn5
Qn6
Qn7
Qn8
Qn9
Vcc
φF
φV
QP5
QD1
Qn10
φR φP φP
BLi
MEMORY CELL

FIG. 5

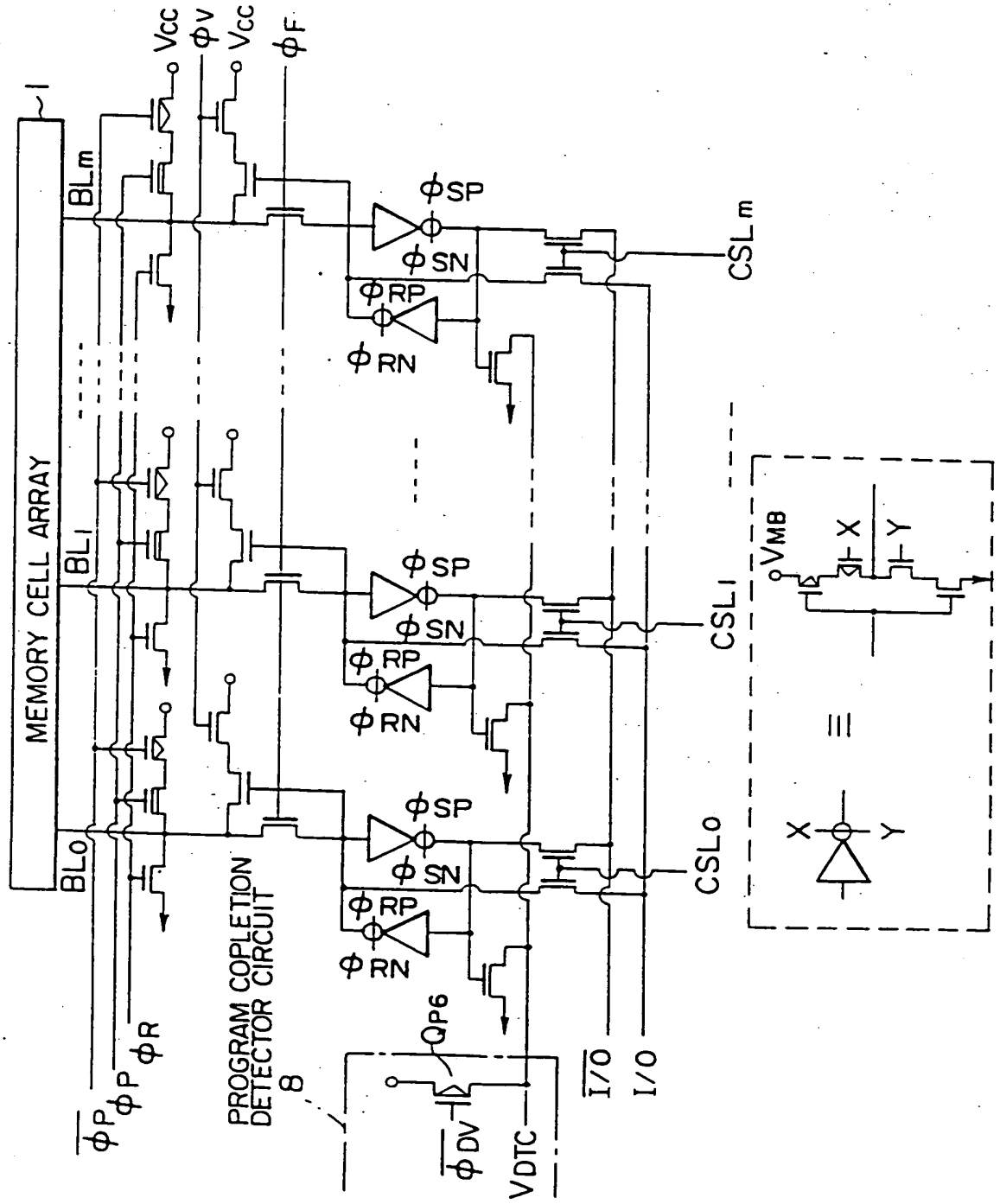

MEMORY CELL ARRAY
BLm
BLI
BLo
Vcc
φV
Vcc
φF
φSP
φSN
φRP
φRN
CSLm
CSLI
CSLo
VMB
X
Y
≡
PROGRAM COPLETION DETECTOR CIRCUIT
8
φP
φP
φR
QP6
φDV
VDTC
I/O
I/O

FIG. 6

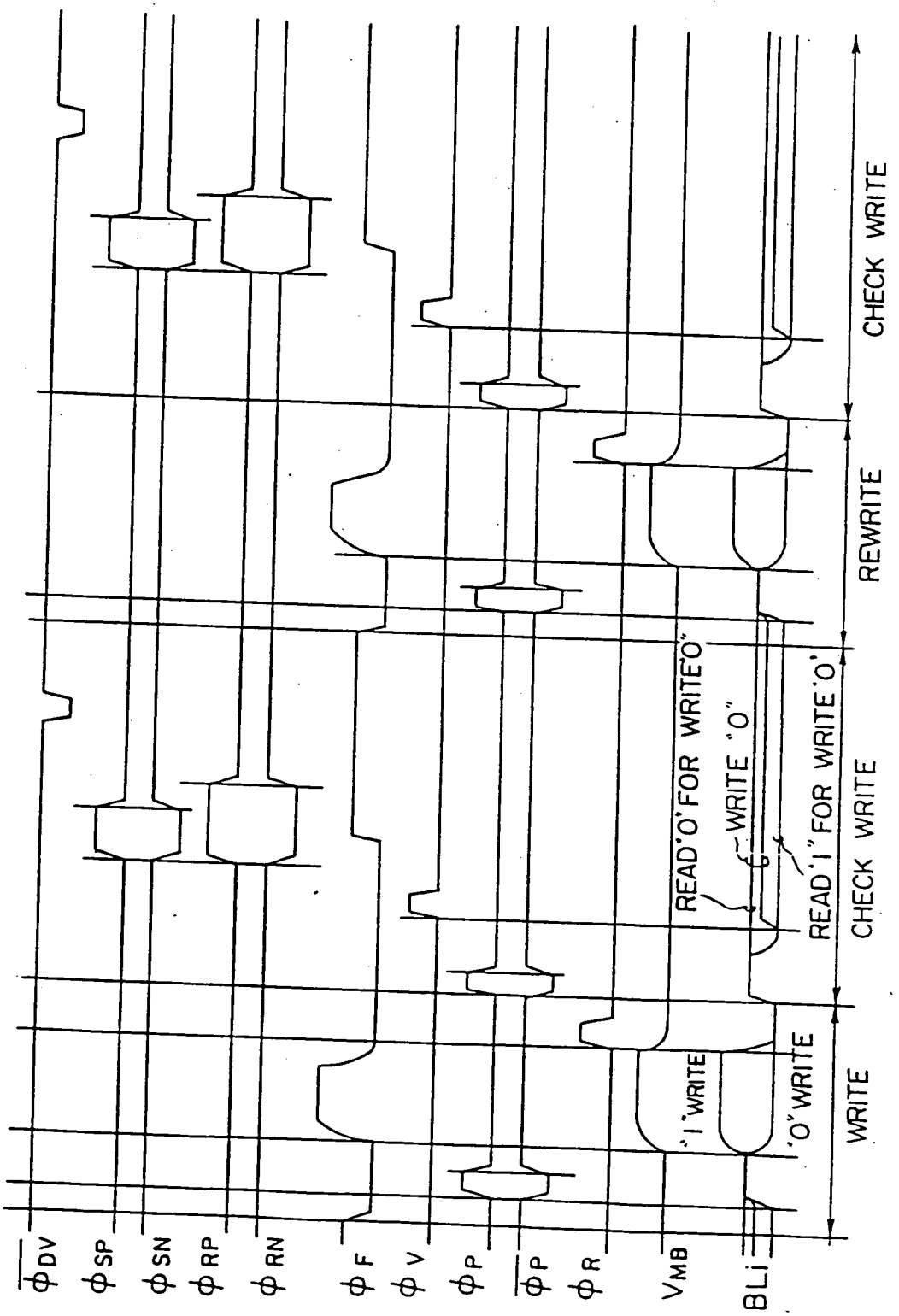

$\overline{\phi DV}$
ϕSP
ϕSN
ϕRP
ϕRN
ϕF
ϕV
ϕP
$\overline{\phi P}$
ϕR
V_{MB}
BLi
WRITE
"0" WRITE
"1" WRITE
CHECK WRITE
READ "1" FOR WRITE "0"
WRITE "0"
READ "0" FOR WRITE "0"
REWRITE
CHECK WRITE

FIG. 7

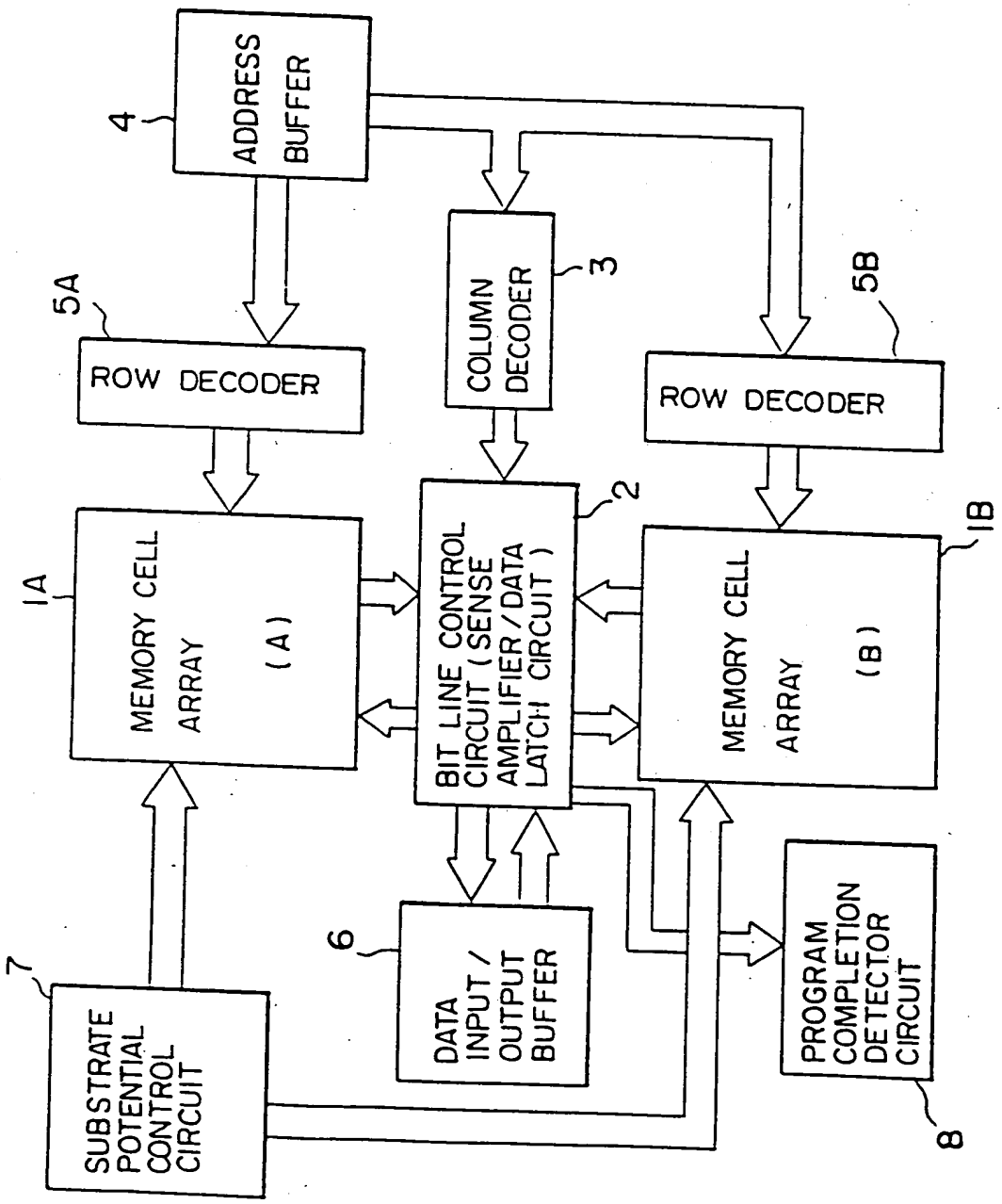

ADDRESS BUFFER
4
COLUMN DECODER
3
5A
ROW DECODER
5B
ROW DECODER
1A
MEMORY CELL ARRAY (A)
BIT LINE CONTROL CIRCUIT (SENSE AMPLIFIER/DATA LATCH CIRCUIT)
2
MEMORY CELL ARRAY (B)
1B
6
DATA INPUT / OUTPUT BUFFER
7
SUBSTRATE POTENTIAL CONTROL CIRCUIT
PROGRAM COMPLETION DETECTOR CIRCUIT
8

FIG. 8

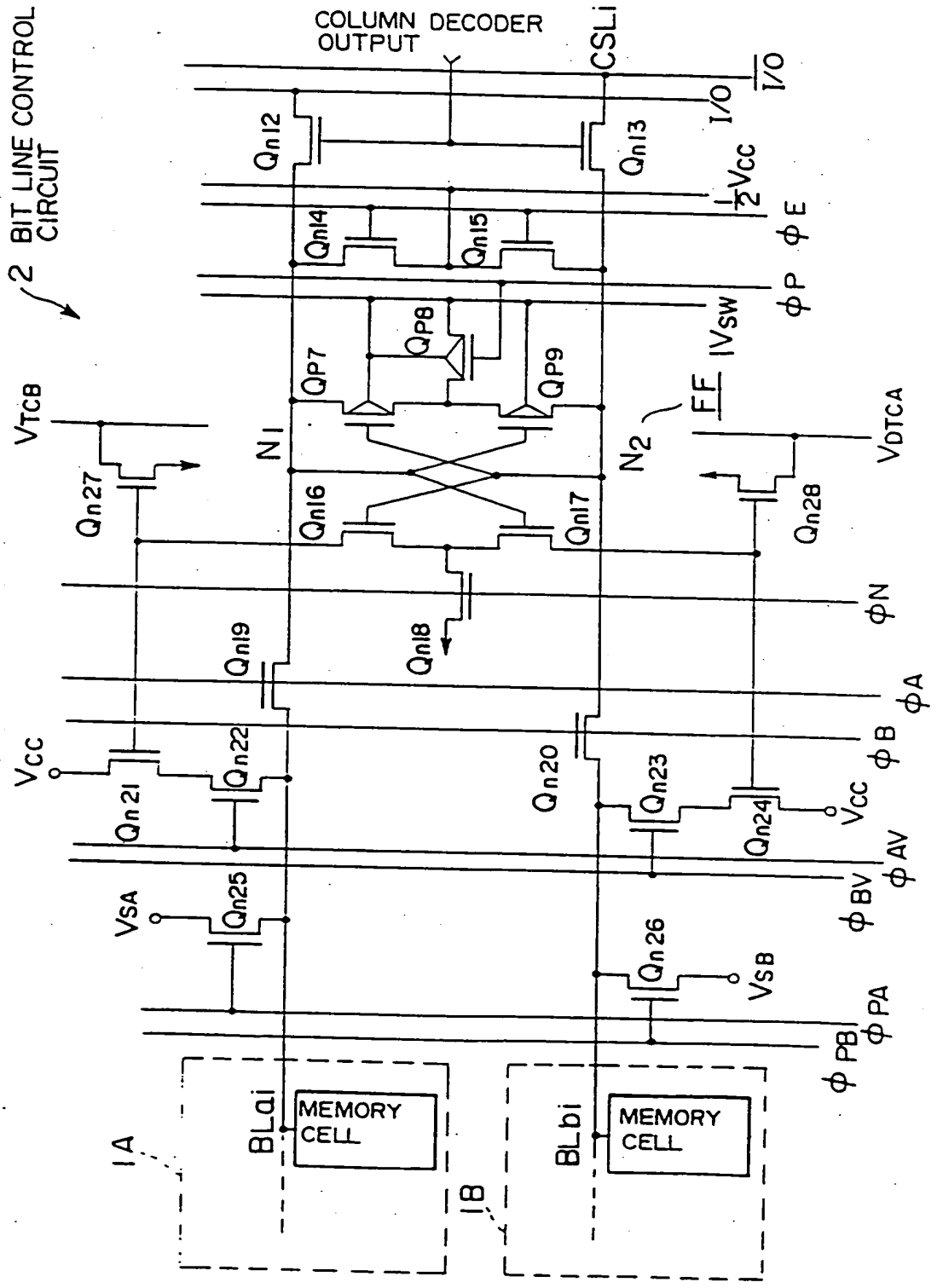

2 BIT LINE CONTROL CIRCUIT
COLUMN DECODER OUTPUT
CSLi
I/O
Qn12
Qn13
1/2Vcc
Qn14
Qn15
φE
φP
VSW
QP7
QP8
QP9
VTCB
N1
N2
F/F
VDTCA
Qn27
Qn16
Qn17
Qn28
φN
Qn19
Qn18
φA
φB
Vcc
Qn21
Qn22
Qn20
Qn23
Qn24
φAV
φBV
VSA
Qn25
Qn26
VSB
φPA
φPB
BLai
MEMORY CELL
BLbi
MEMORY CELL
IA
IB

FIG. 9

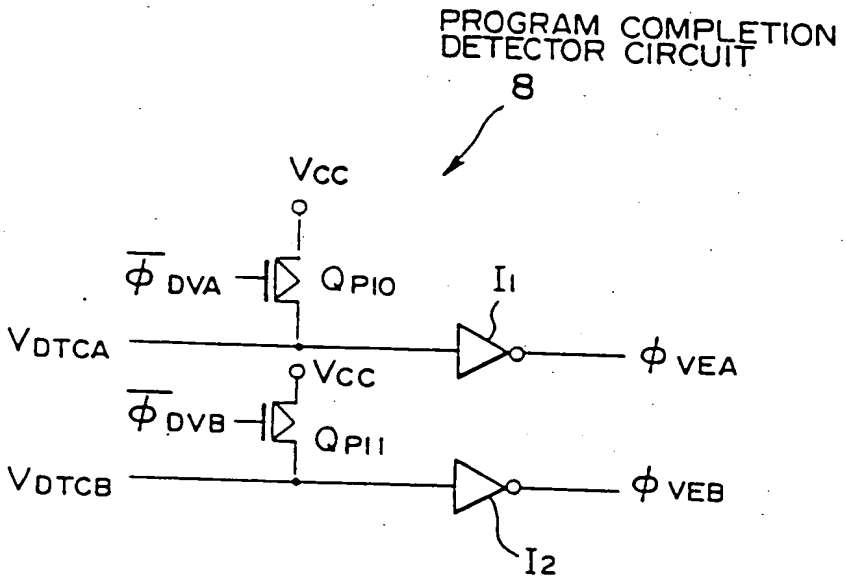

PROGRAM COMPLETION
DETECTOR CIRCUIT
8
Vcc
$\overline{\phi}$DVA
QP10
I1
VDTCA
ϕVEA
Vcc
$\overline{\phi}$DVB
QP11
VDTCB
ϕVEB
I2

FIG.10

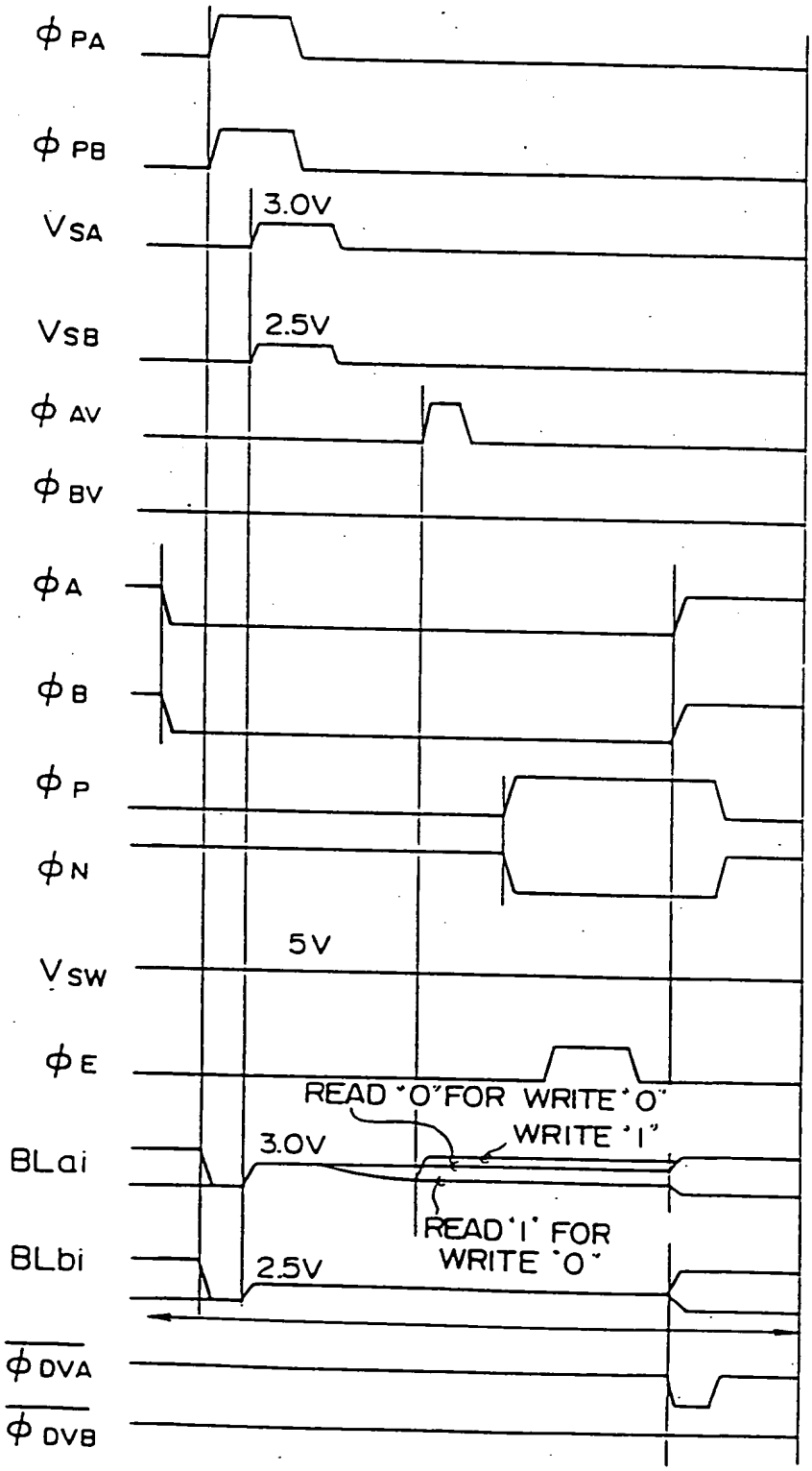

φ PA
φ PB
VSA
3.0V
VSB
2.5V
φ AV
φ BV
φ A
φ B
φ P
φ N
VSW
5V
φ E
READ "0" FOR WRITE "0"
WRITE "1"
BLai
3.0V
READ "1" FOR
WRITE "0"
BLbi
2.5V
φ DVA
φ DVB

FIG. 11

FIG. 12(a)

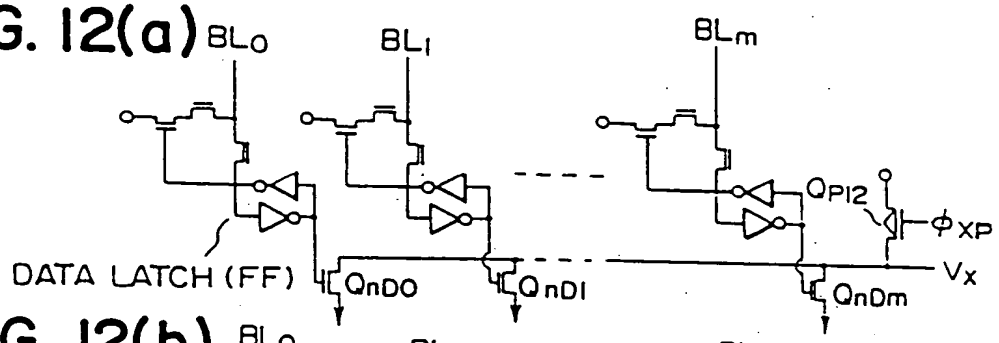


FIG. 12(b)

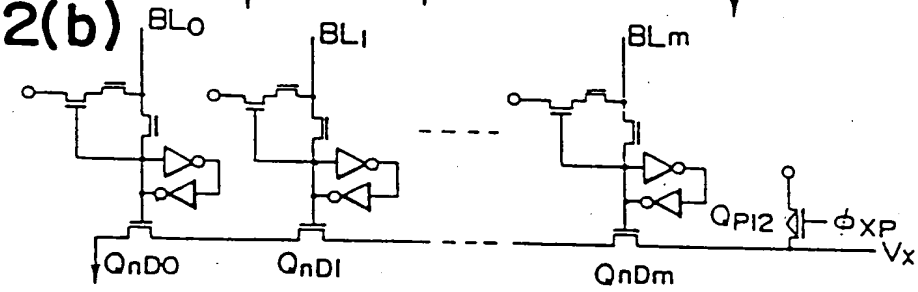


FIG. 12(c)

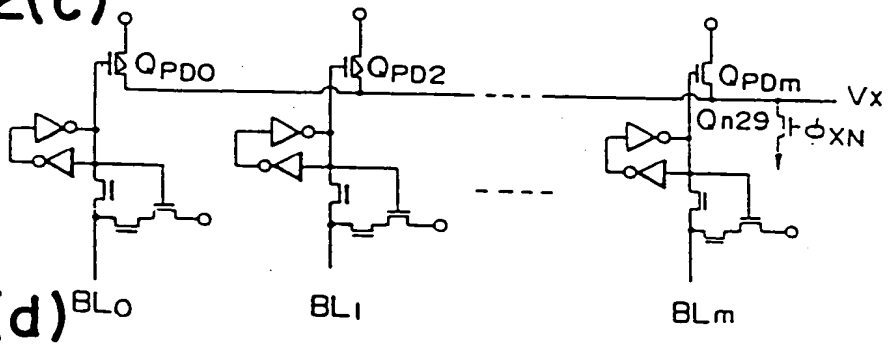


FIG. 12(d)

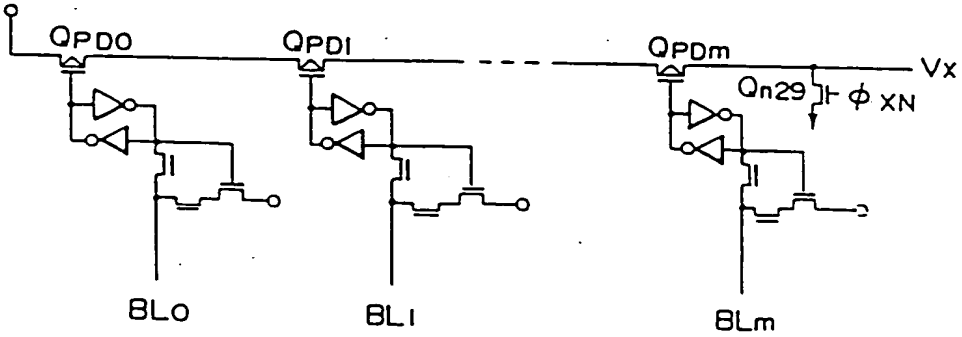


FIG. 13(a)

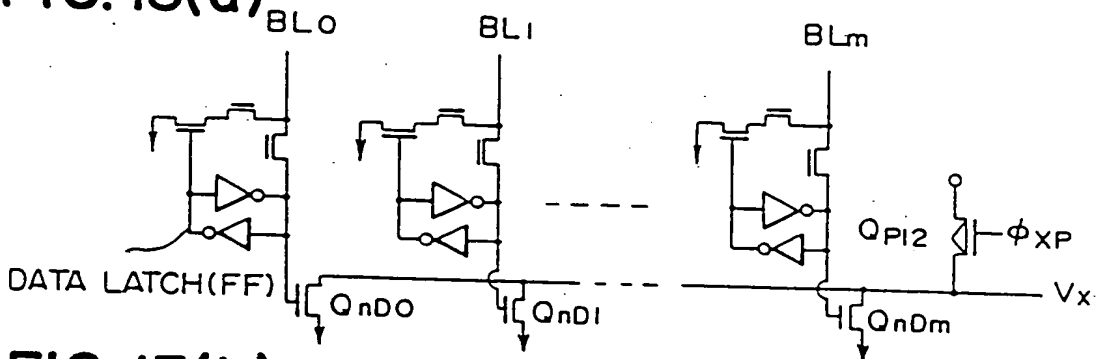


FIG. 13(b)

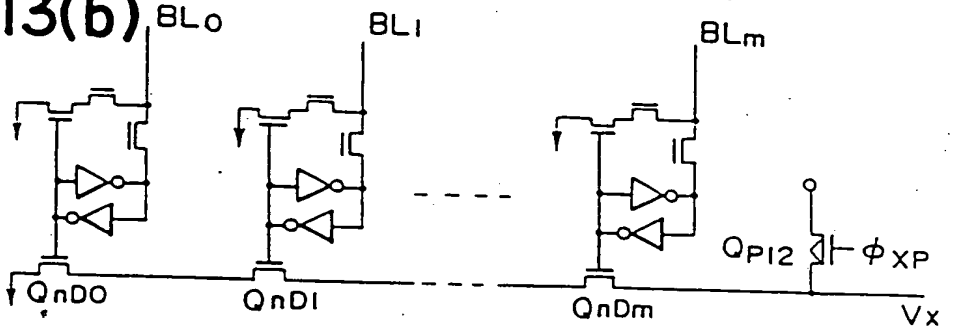


FIG. 13(c)

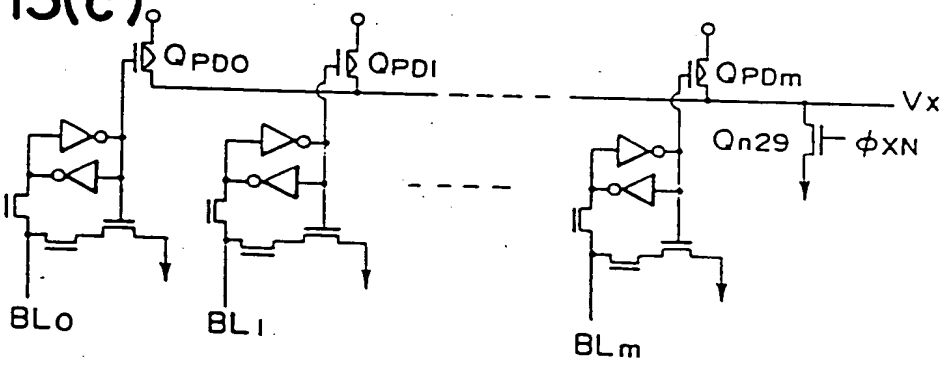
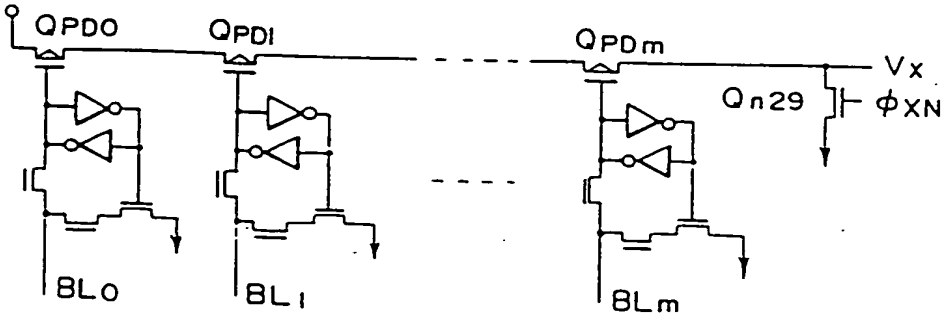


FIG. 13(d)



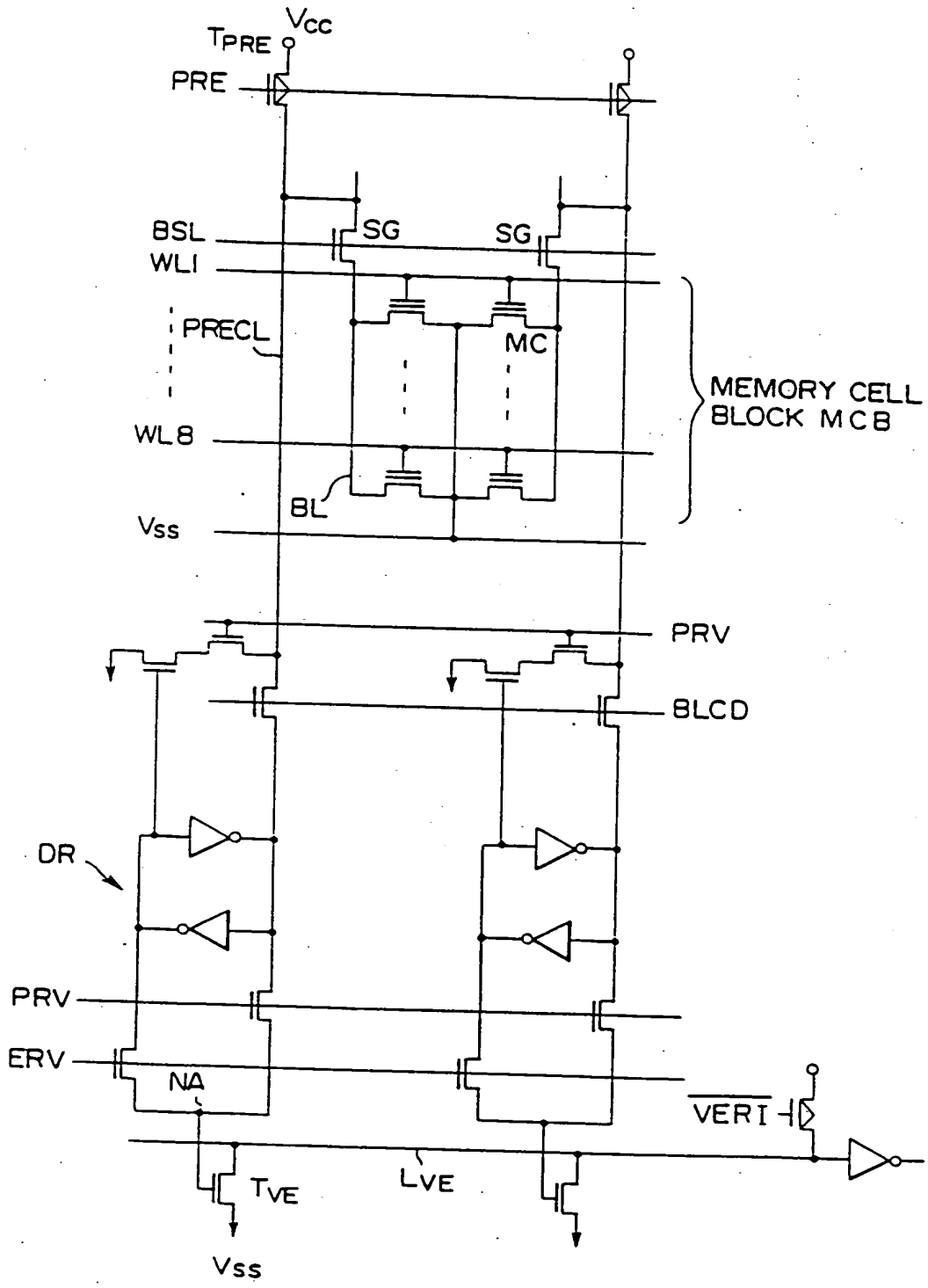

Vcc
TPRE
PRE
BSL
WLI
SG
SG
PRECL
MC
MEMORY CELL
BLOCK MCB
WL8
BL
Vss
PRV
BLCD
DR
PRV
ERV
NA
VERI
TVE
LVE
Vss

FIG. 14

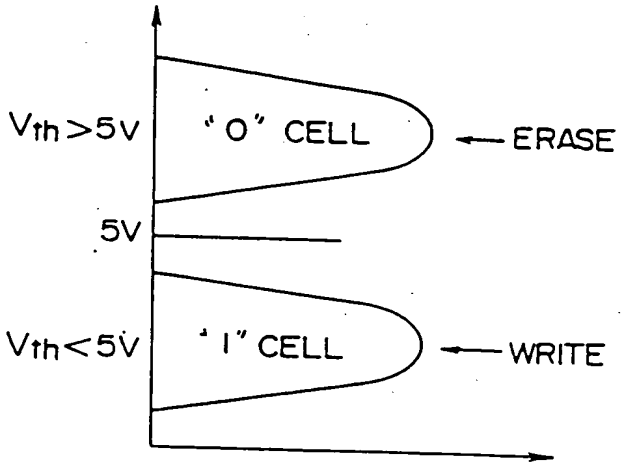


FIG. 15

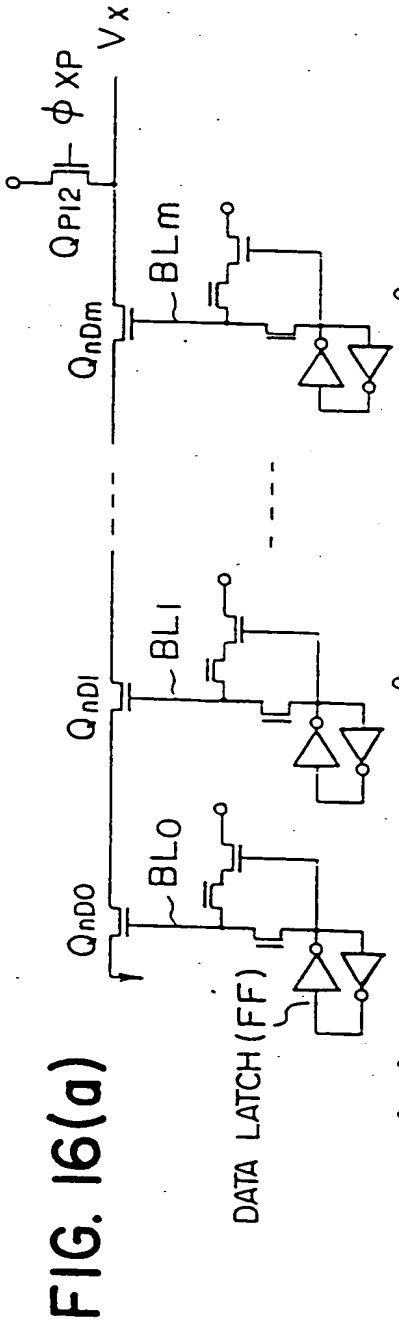


FIG. 16(a)

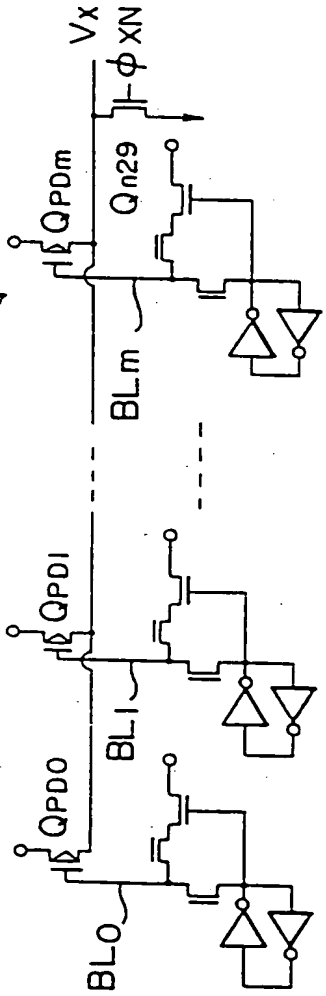


FIG. 16(b)

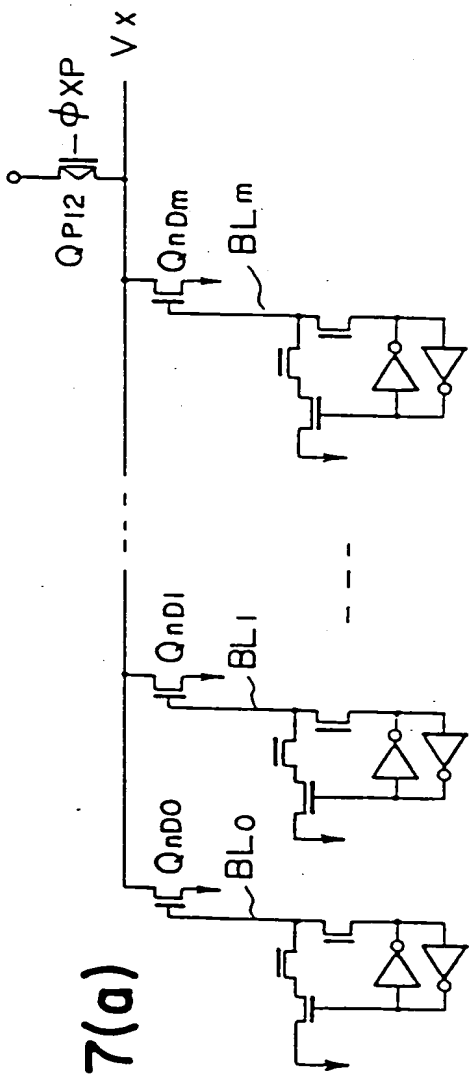


FIG. 17(a)

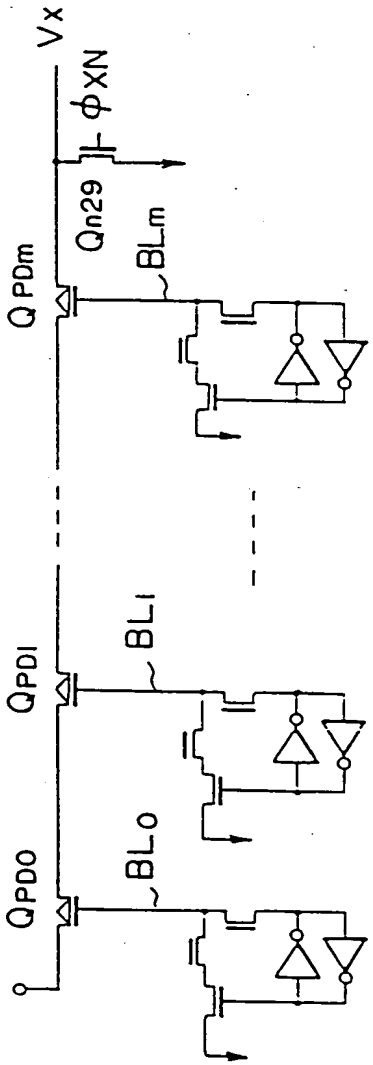


FIG. 17(b)

FIG. 18(a)

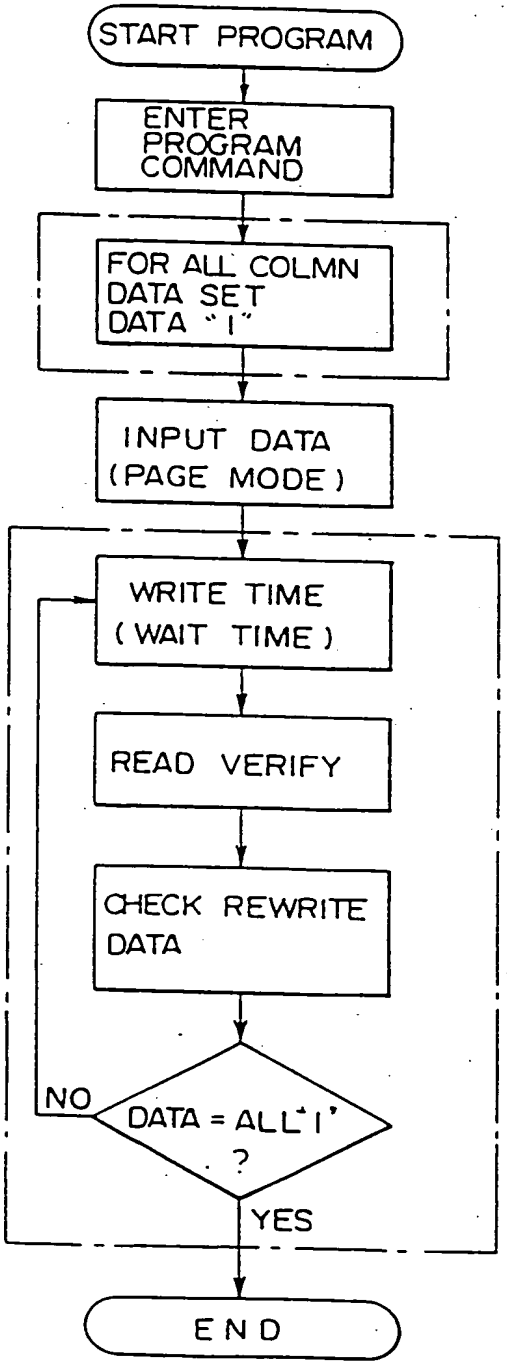


FIG. 18(b)

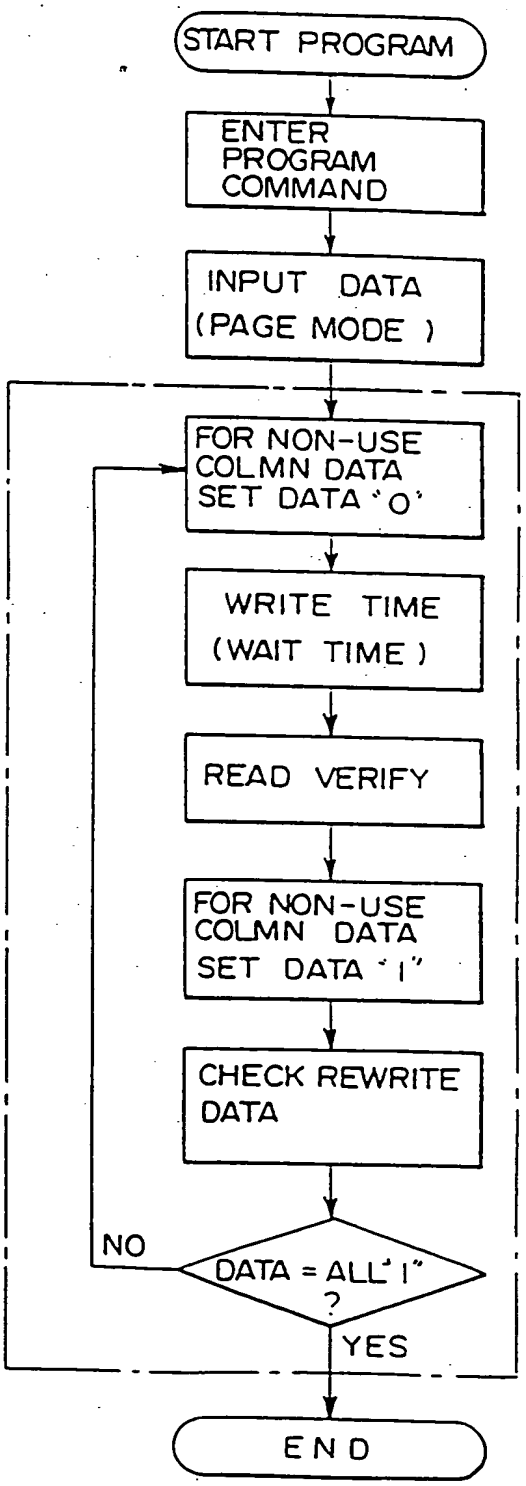


FIG. 19(a)

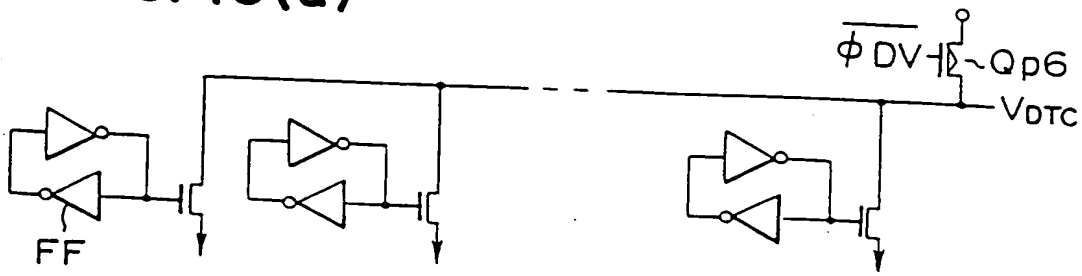


FIG. 19(b)

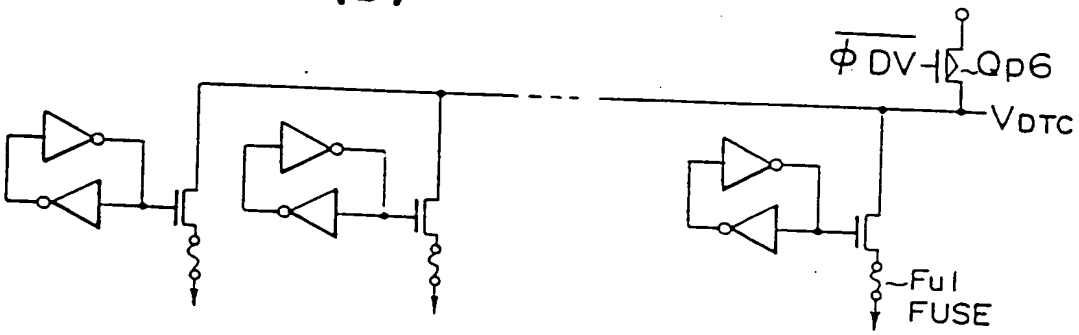


FIG. 19(c)

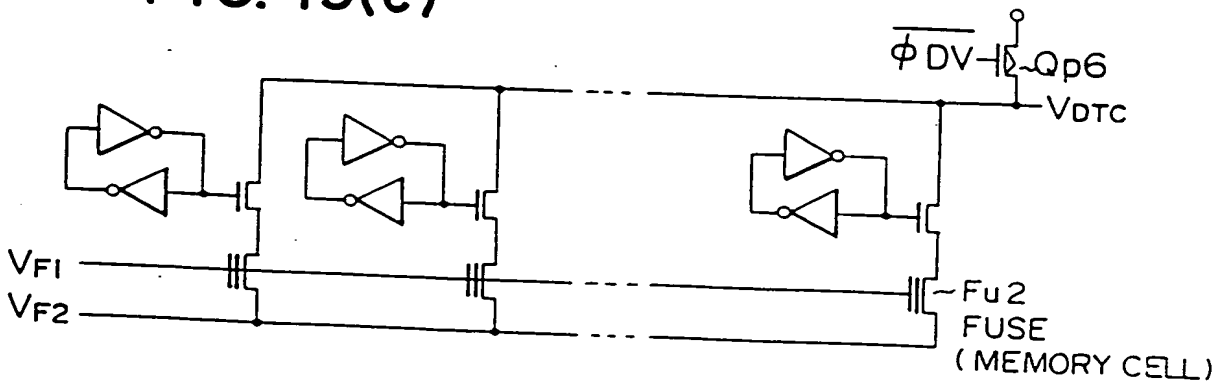


FIG. 20(a)

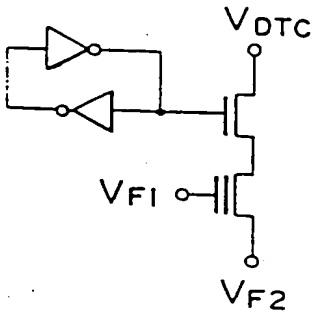


FIG. 20(b)

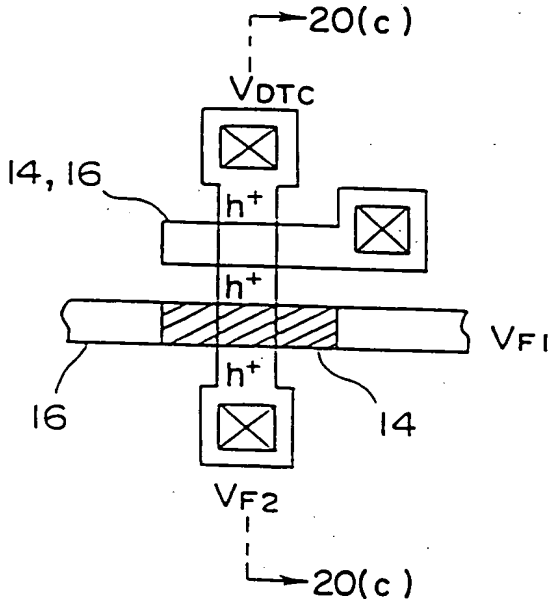


FIG. 20(c)

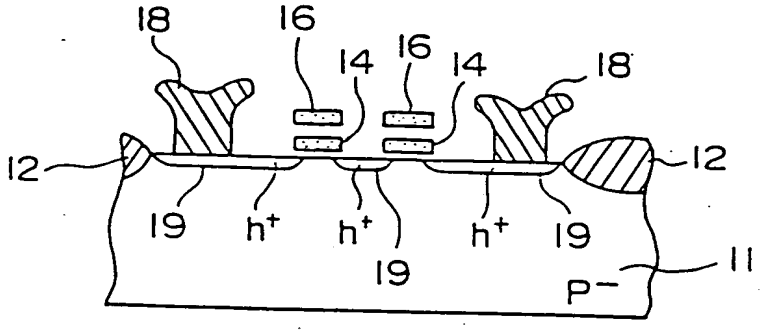


FIG. 21(a)

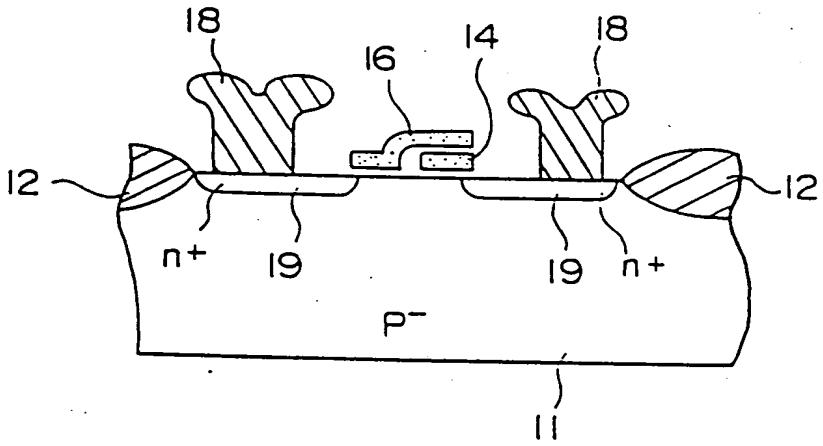


FIG. 21(b)

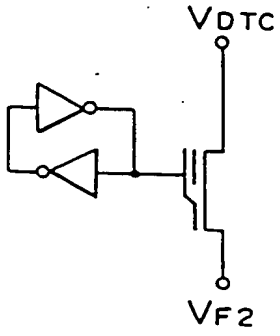
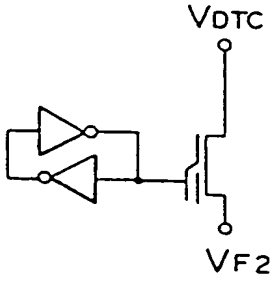


FIG. 21(c)



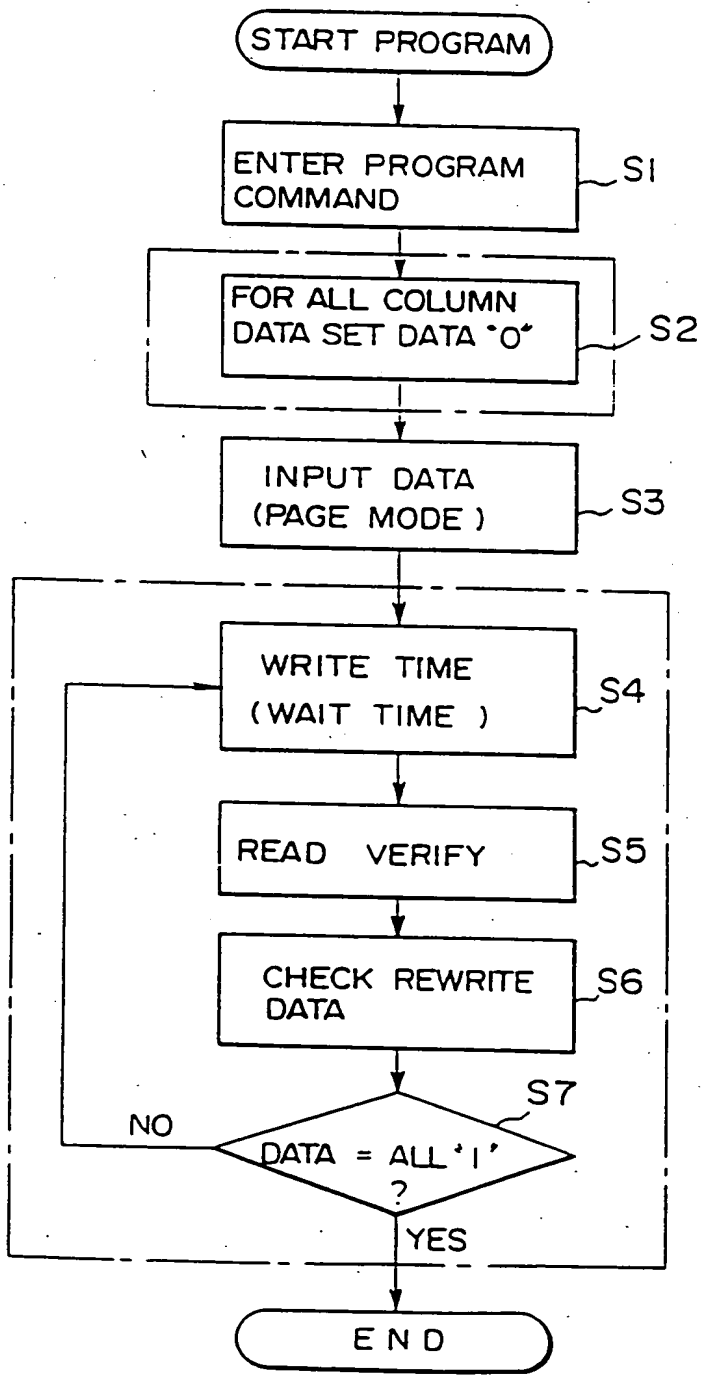

START PROGRAM
ENTER PROGRAM COMMAND
S1
FOR ALL COLUMN DATA SET DATA "0"
S2
INPUT DATA (PAGE MODE)
S3
WRITE TIME (WAIT TIME)
S4
READ VERIFY
S5
CHECK REWRITE DATA
S6
S7
NO
DATA = ALL '1' ?
YES
END

FIG. 22

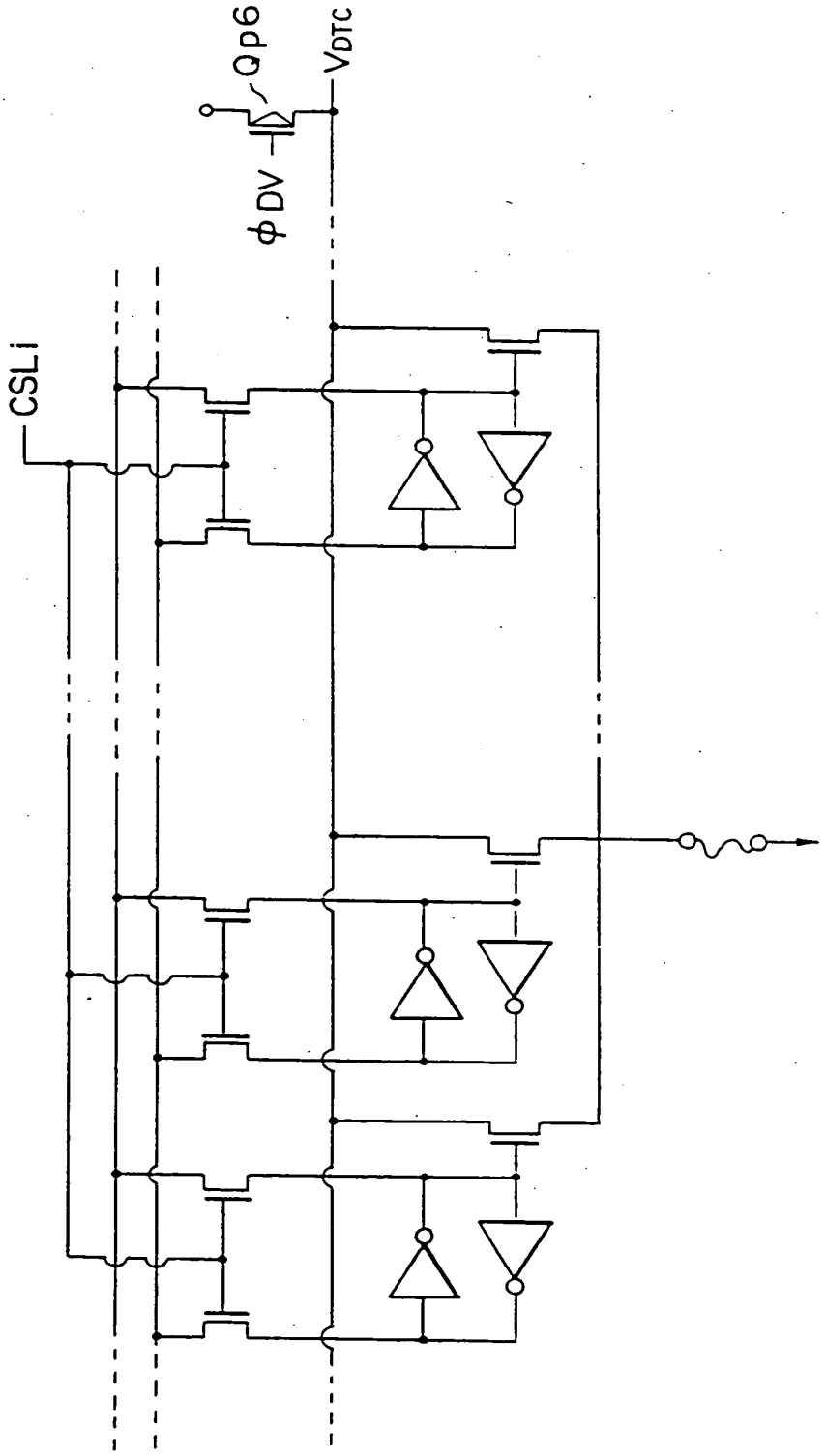


FIG. 23

FIG. 24(a)

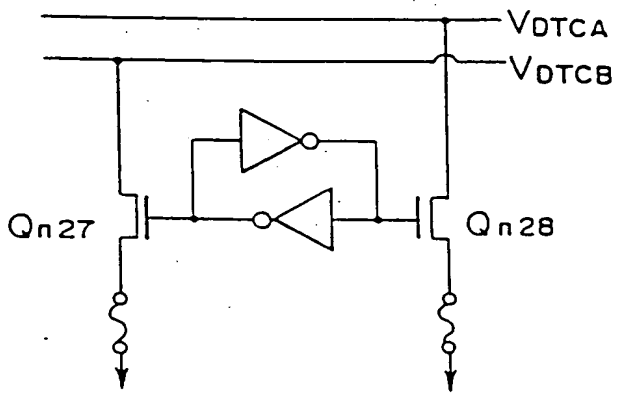


FIG. 24(b)

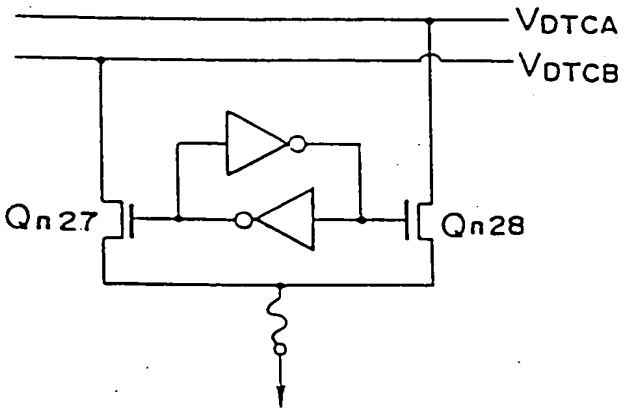


FIG. 25(a)

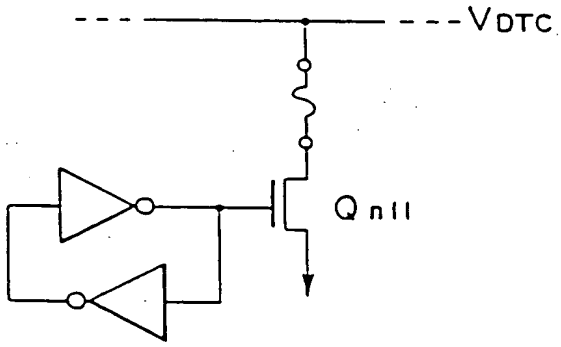


FIG. 25(b)

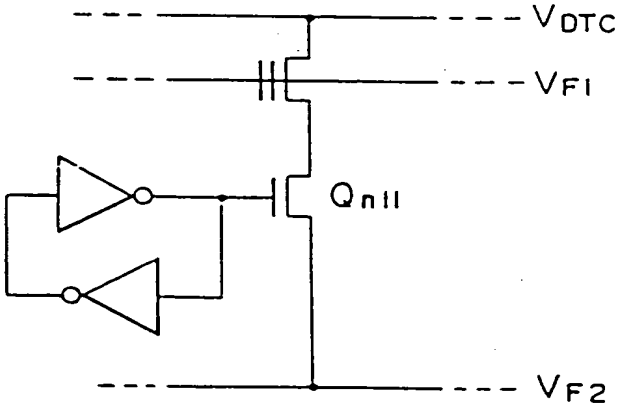


FIG. 26(a)

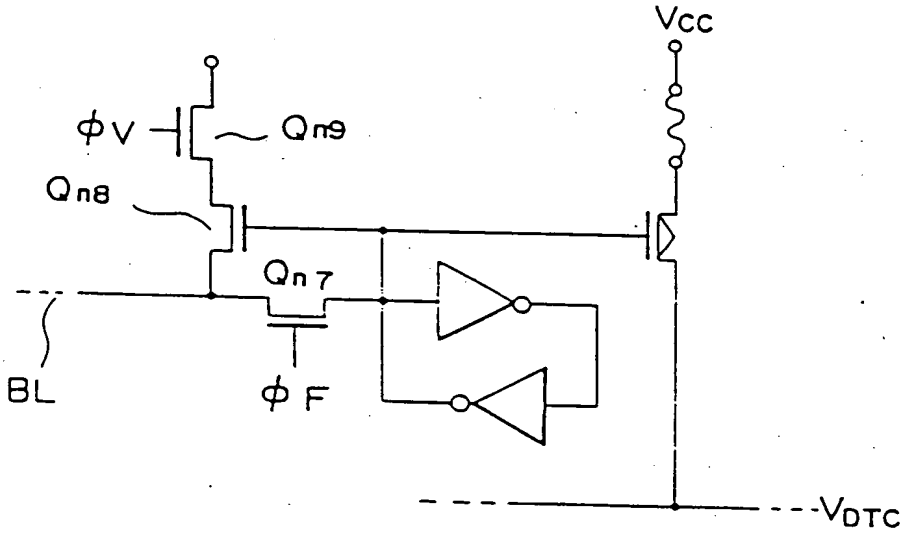


FIG. 26(b)

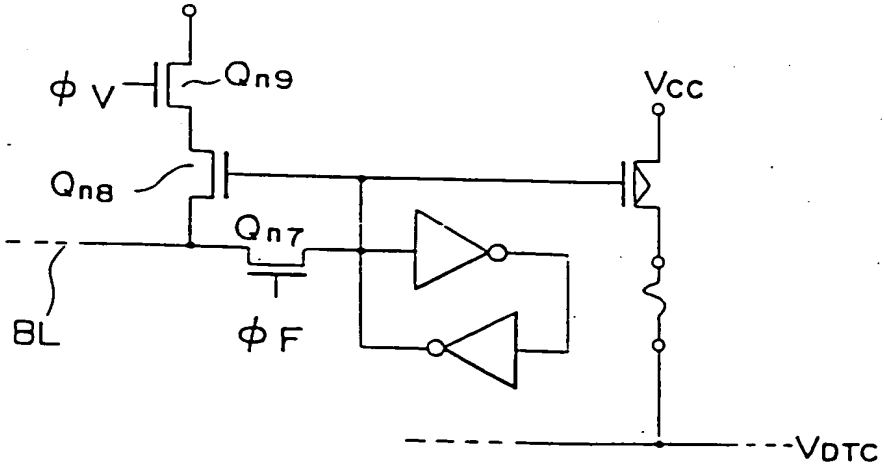


FIG. 27(a)

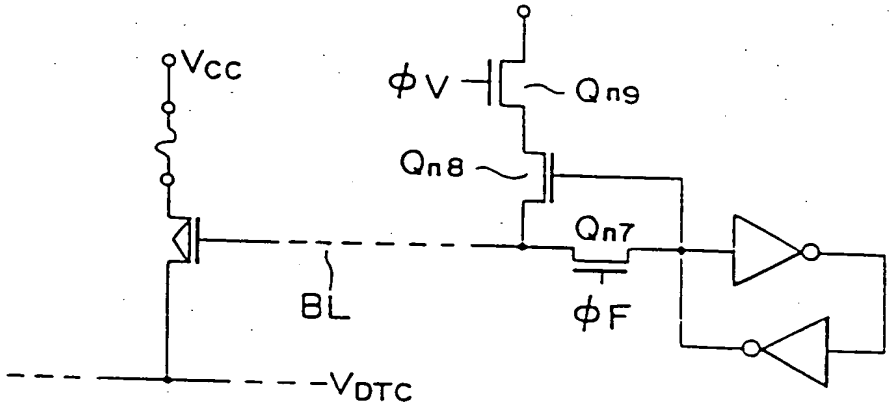


FIG. 27(b)

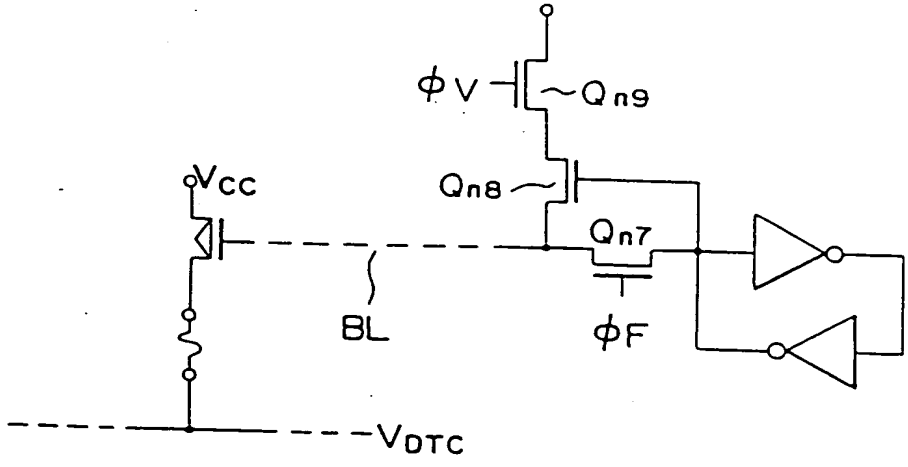


FIG. 28(b)

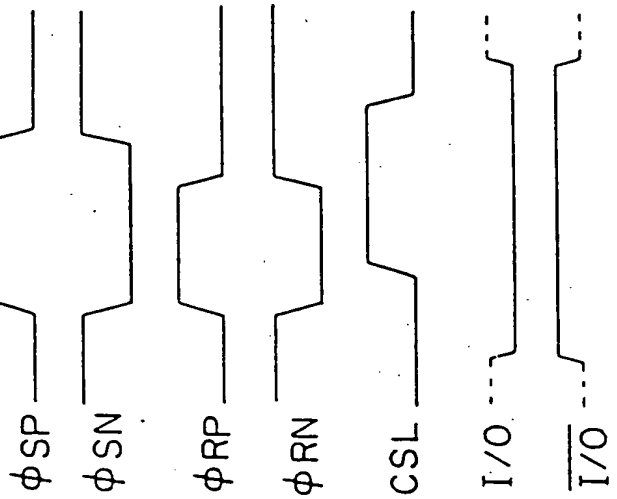
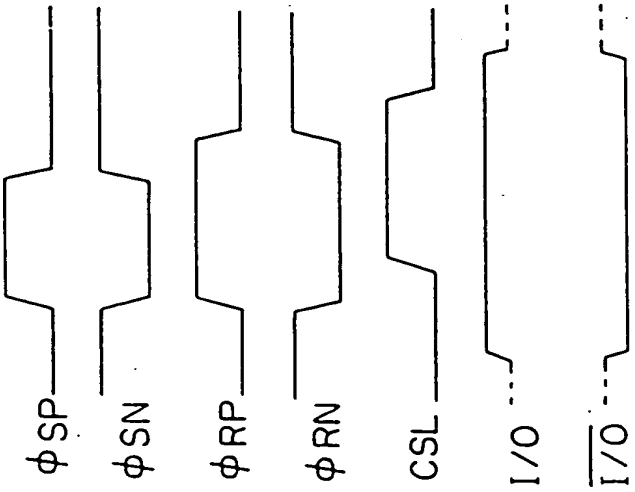


FIG. 28(a)



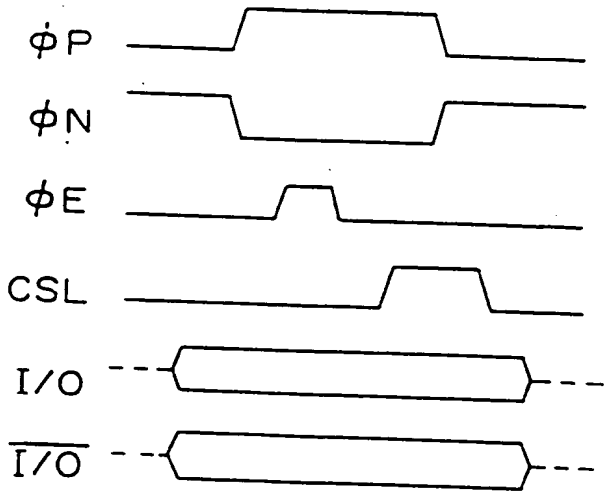


FIG. 29

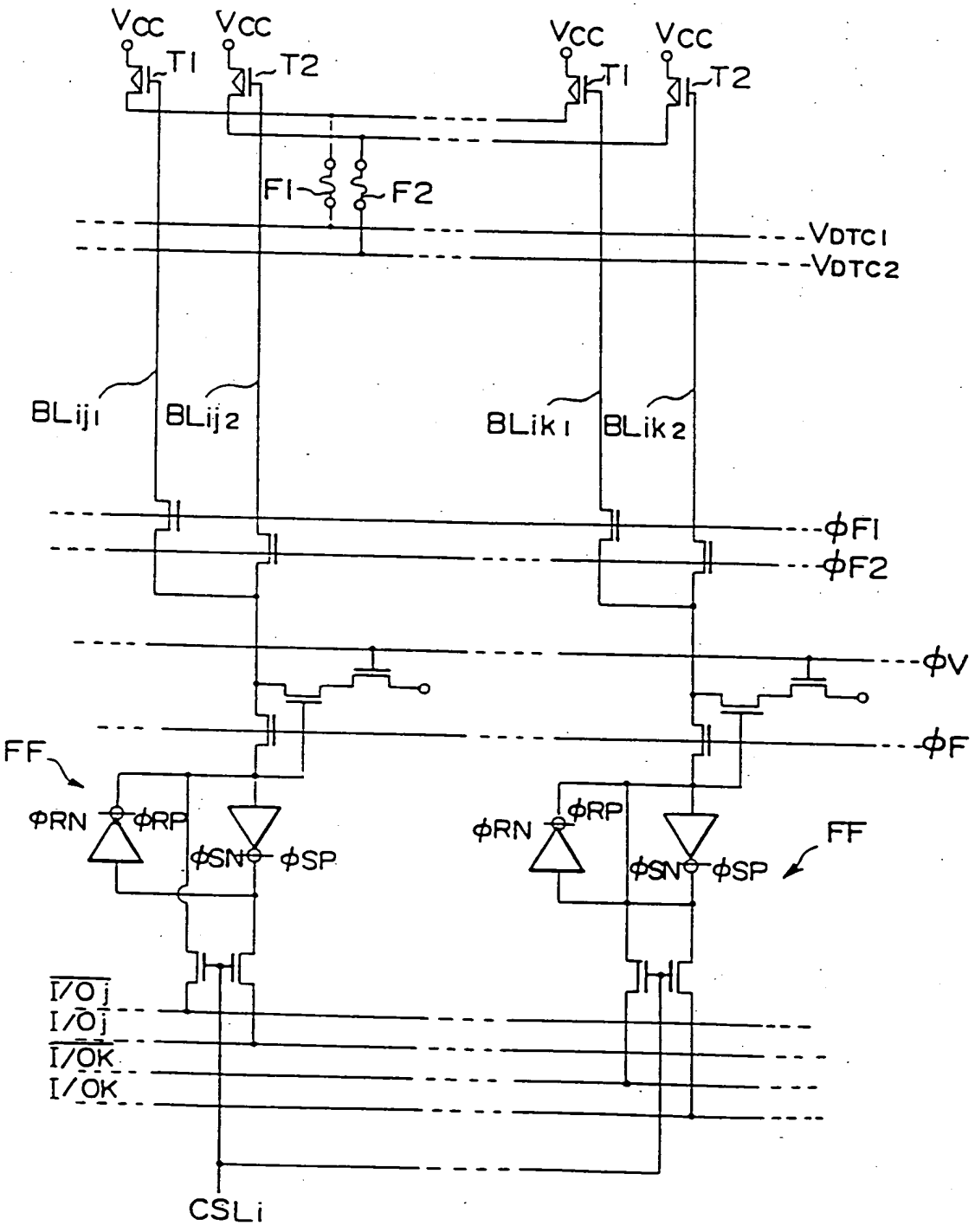

Vcc
Vcc
Vcc
Vcc
T1
T2
T1
T2
F1
F2
VDTC1
VDTC2
BLij1
BLij2
BLik1
BLik2
φF1
φF2
φV
φF
FF
φRN
φRP
φSN
φSP
φRN
φRP
φSN
φSP
FF
I/Oj
I/Oj
I/OK
I/OK
CSLi

FIG. 30

FIG. 31(a)

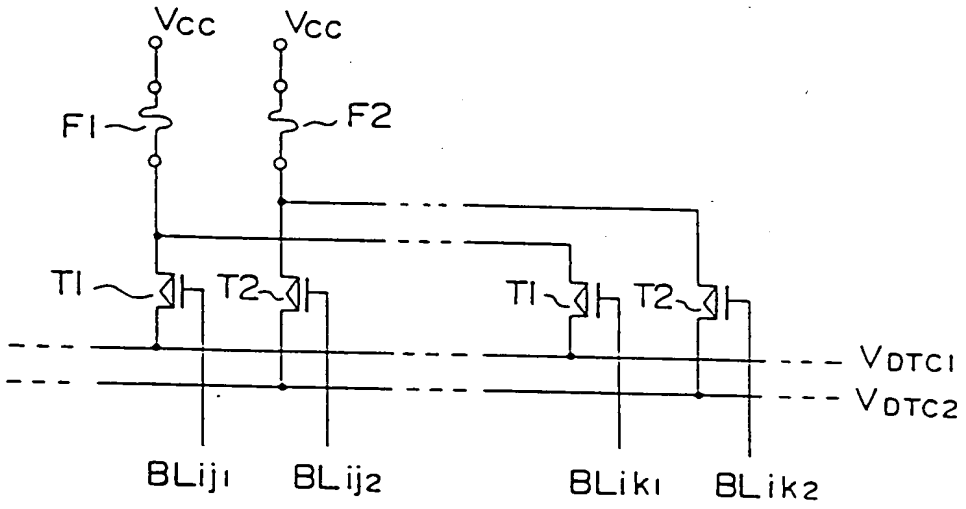
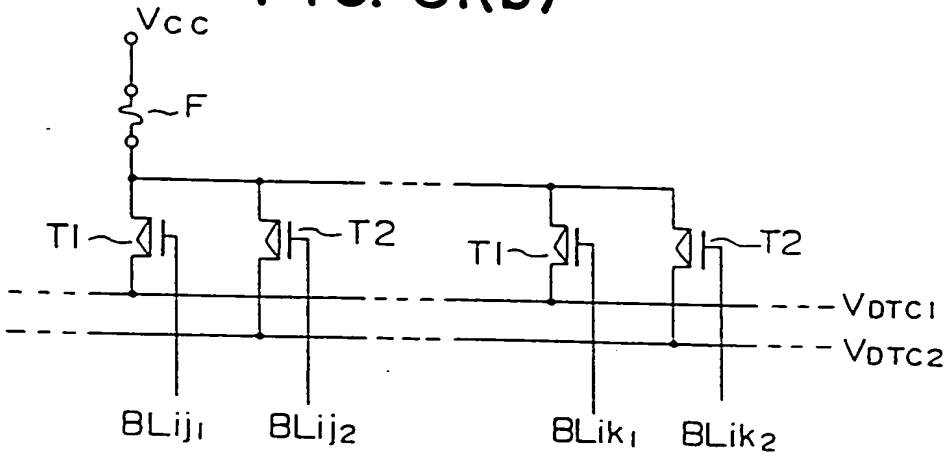


FIG. 31(b)



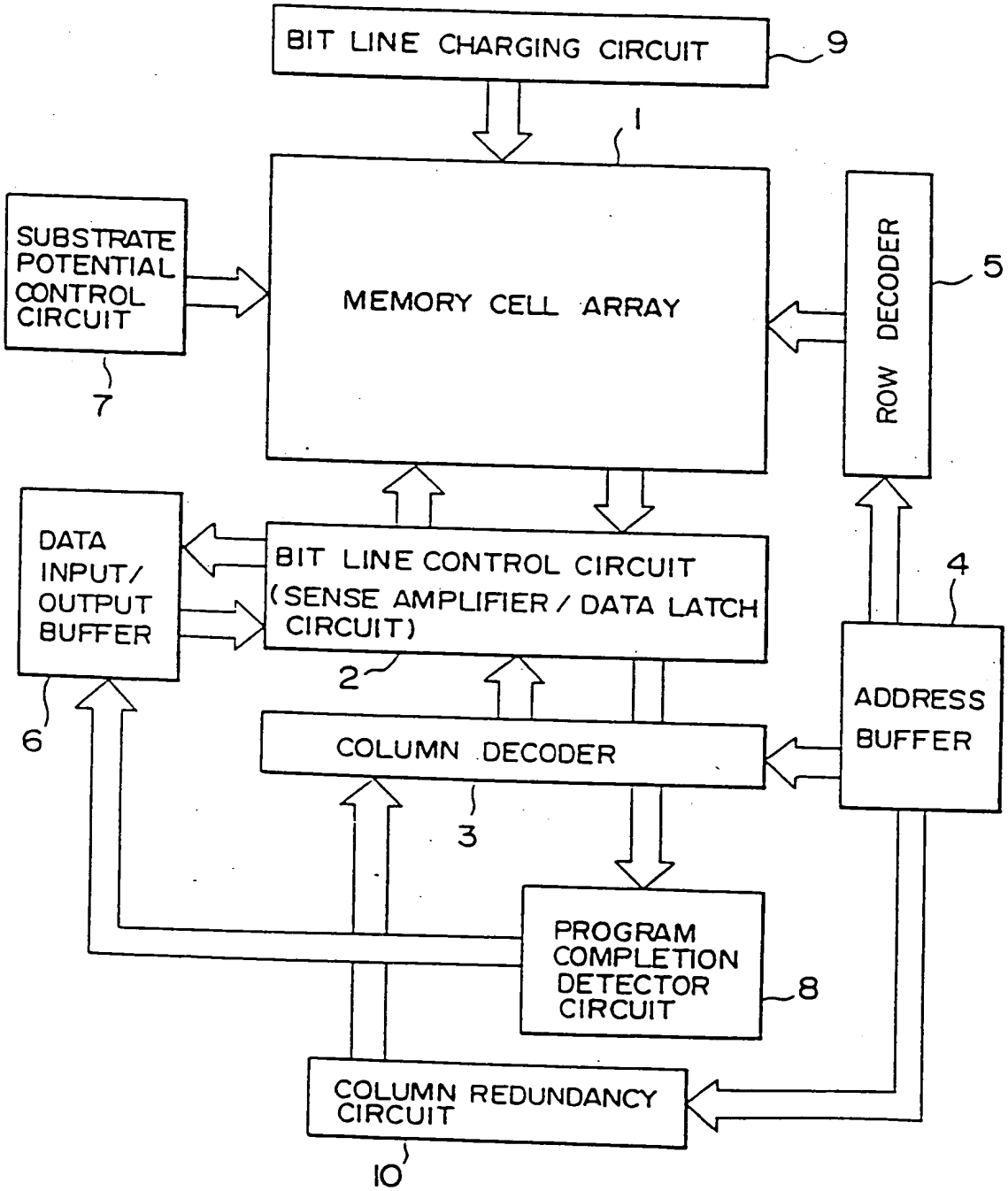

BIT LINE CHARGING CIRCUIT
9
1
SUBSTRATE POTENTIAL CONTROL CIRCUIT
7
MEMORY CELL ARRAY
ROW DECODER
5
DATA INPUT/ OUTPUT BUFFER
6
BIT LINE CONTROL CIRCUIT (SENSE AMPLIFIER / DATA LATCH CIRCUIT)
2
4
ADDRESS BUFFER
COLUMN DECODER
3
PROGRAM COMPLETION DETECTOR CIRCUIT
8
COLUMN REDUNDANCY CIRCUIT
10

FIG. 32

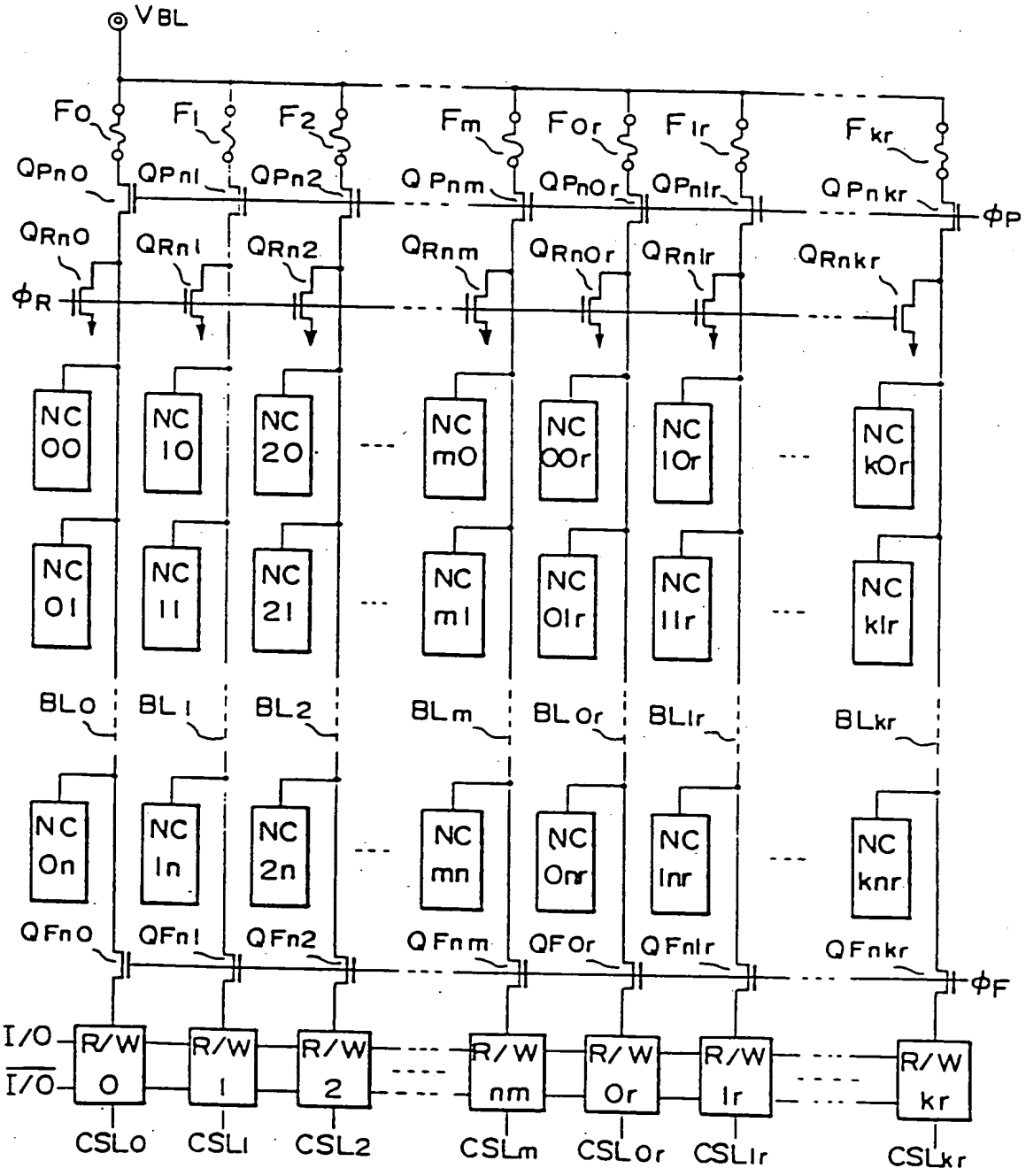

VBL
F0
F1
F2
Fm
For
Flr
Fkr
QPn0
QPn1
QPn2
QPnm
QPn0r
QPn1r
QPnkr
φP
QRn0
QRn1
QRn2
QRnm
QRn0r
QRn1r
QRnkr
φR
NC 00
NC 10
NC 20
NC m0
NC 00r
NC 10r
NC k0r
NC 01
NC 11
NC 21
NC m1
NC 01r
NC 11r
NC k1r
BL0
BL1
BL2
BLm
BL0r
BL1r
BLkr
NC 0n
NC 1n
NC 2n
NC mn
NC 0nr
NC 1nr
NC knr
QFn0
QFn1
QFn2
QFnm
QF0r
QFn1r
QFnkr
φF
I/O
I/O
R/W 0
R/W 1
R/W 2
R/W nm
R/W 0r
R/W 1r
R/W kr
CSL0
CSL1
CSL2
CSLm
CSL0r
CSL1r
CSLkr

FIG. 33

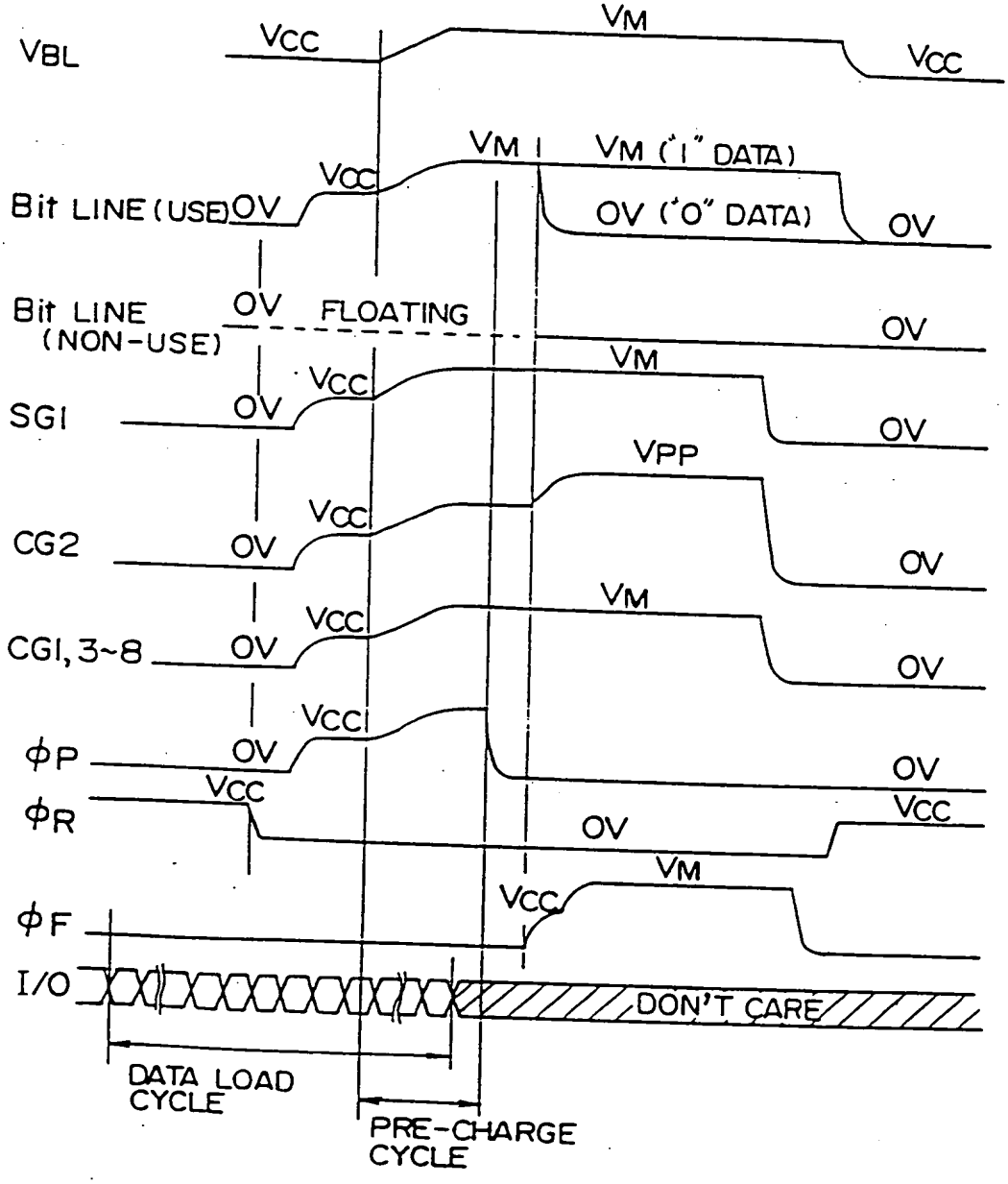

VBL
Vcc
VM
Vcc
Bit LINE (USE)
OV
Vcc
VM
VM ("1" DATA)
OV ("0" DATA)
OV
Bit LINE
(NON-USE)
OV
FLOATING
OV
SGI
OV
Vcc
VM
OV
CG2
OV
Vcc
VPP
OV
CGI, 3~8
OV
Vcc
VM
OV
φP
OV
Vcc
OV
φR
Vcc
OV
Vcc
φF
VM
Vcc
I/O
DON'T CARE
DATA LOAD
CYCLE
PRE-CHARGE
CYCLE

FIG. 34

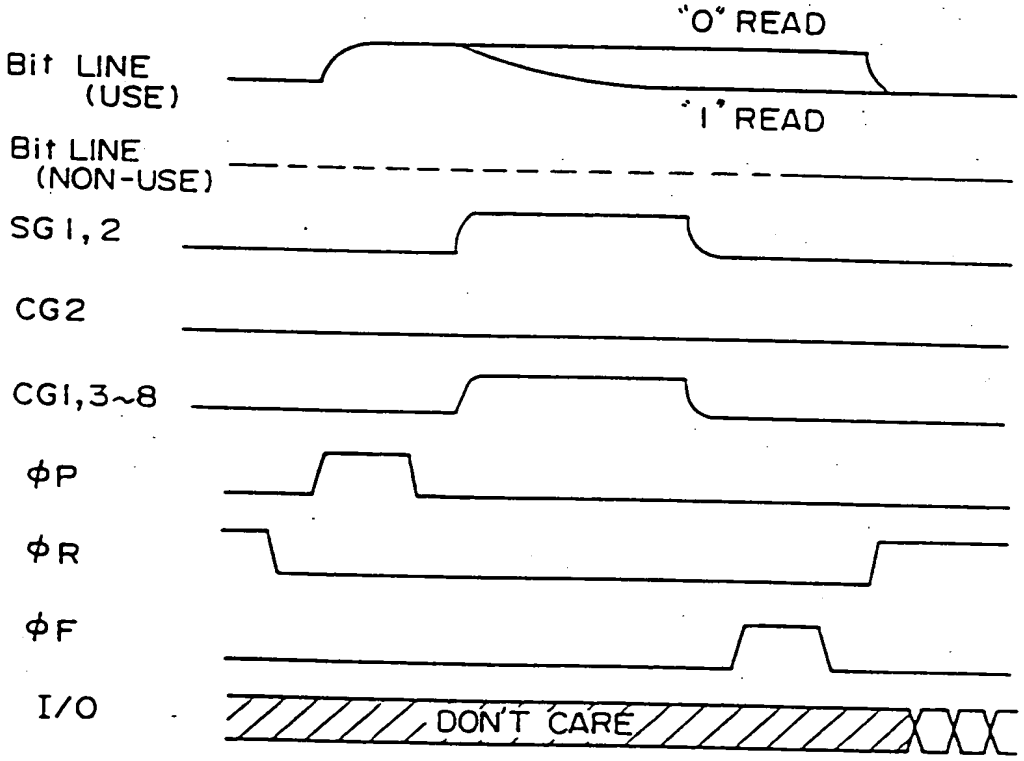

"0" READ
Bit LINE
(USE)
"1" READ
Bit LINE
(NON-USE)
SG1,2
CG2
CG1,3~8
φP
φR
φF
I/O
DON'T CARE

FIG.35

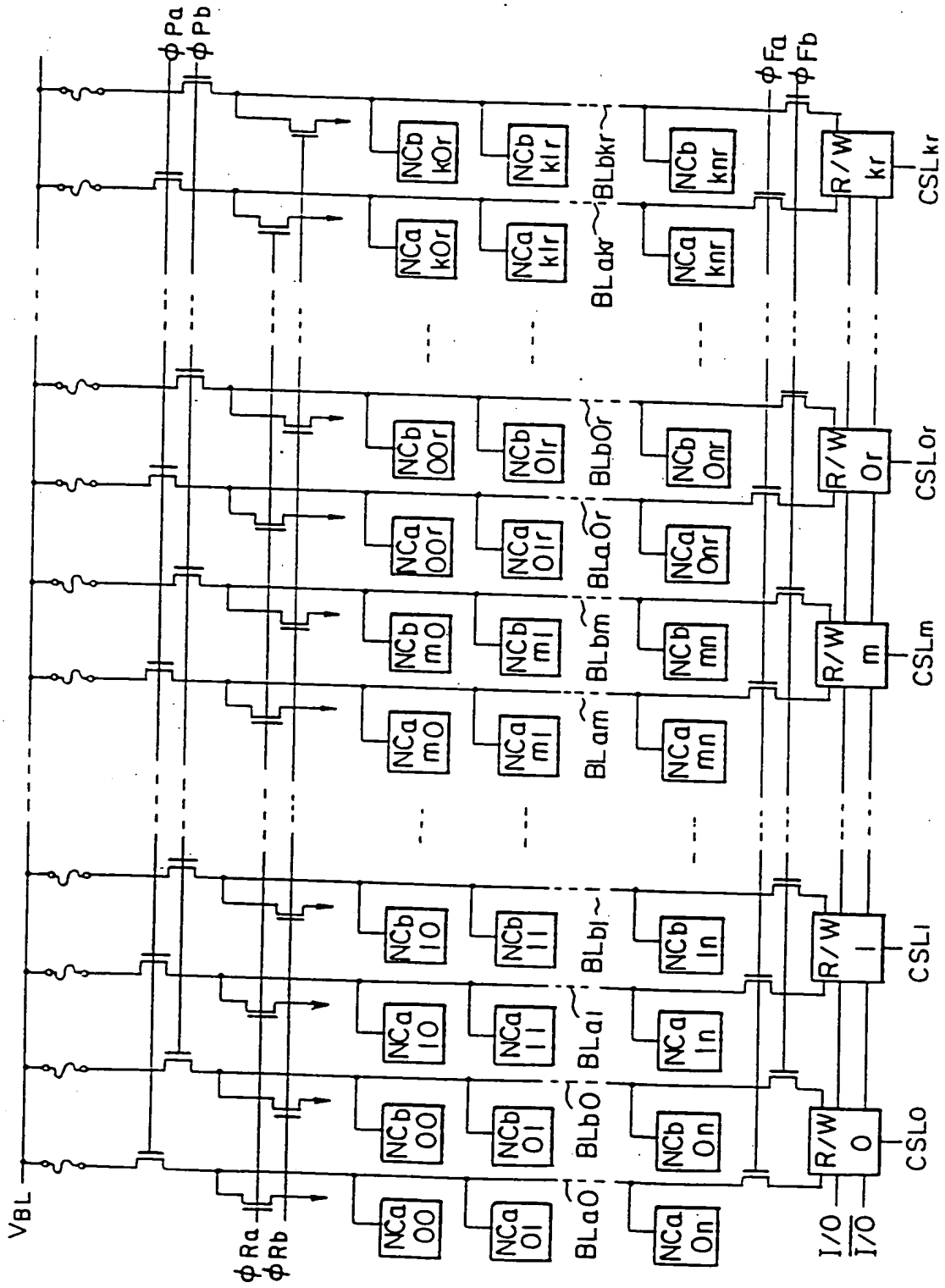

φPa
φPb
φFa
φFb
NCb kOr
NCb klr
NCb knr
R/W kr
CSLkr
BLbkr
BLakr
NCa kOr
NCa klr
NCa knr
NCb OOr
NCb Olr
NCb Onr
R/W Or
CSLOr
BLbOr
BLaOr
NCa OOr
NCa Olr
NCa Onr
NCb mO
NCb ml
NCb mn
R/W m
CSLm
BLbm
BLam
NCa mO
NCa ml
NCa mn
NCb lO
NCb ll
NCb ln
R/W l
CSLl
BLbl
BLal
NCa lO
NCa ll
NCa ln
NCb OO
NCb Ol
NCb On
R/W O
CSLO
BLbO
BLaO
NCa OO
NCa Ol
NCa On
VBL
φRa
φRb
I/O
I/O

FIG.36

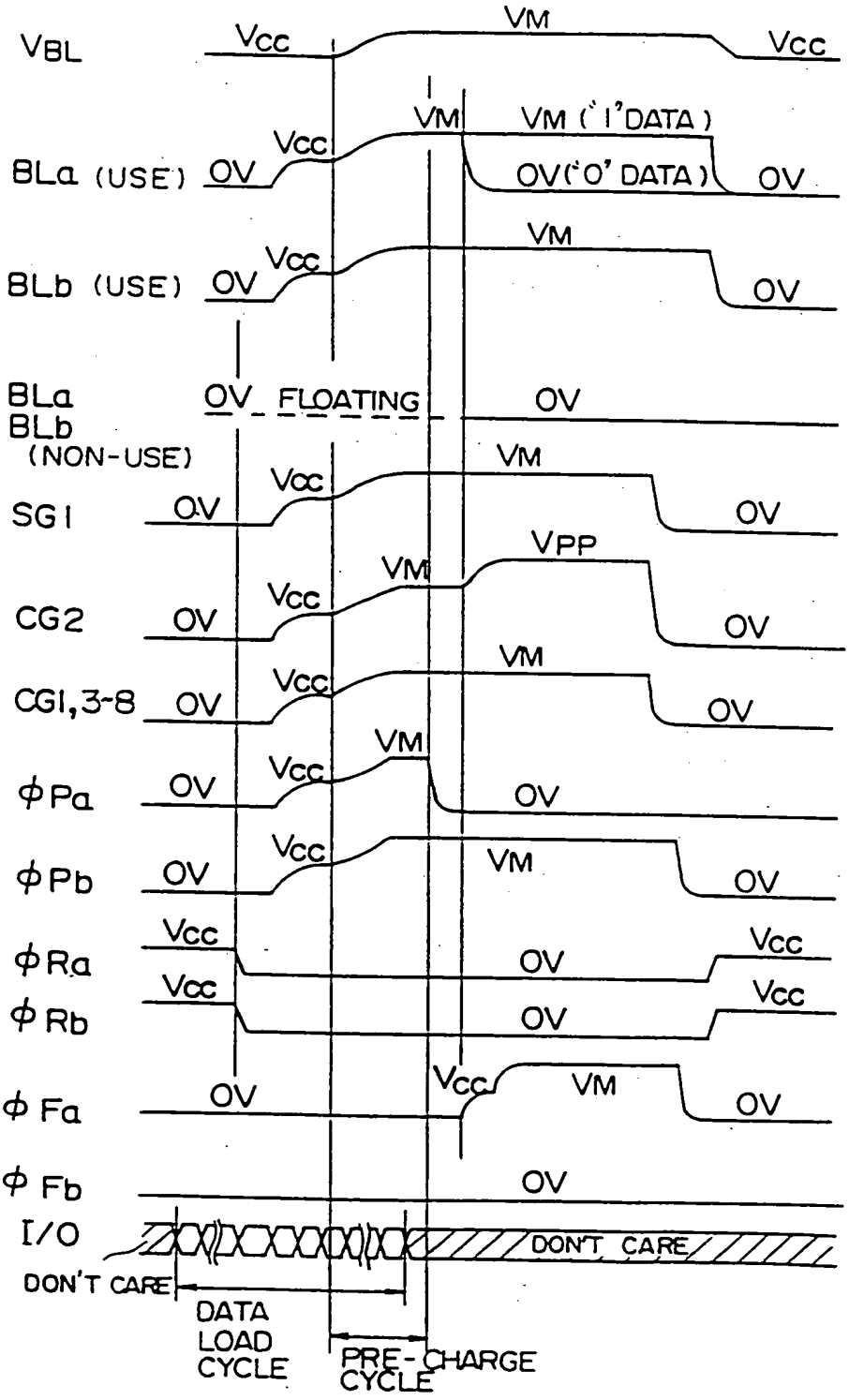

VBL
Vcc
VM
Vcc
BLa (USE)
OV
Vcc
VM
VM ('1' DATA)
OV ('0' DATA)
OV
BLb (USE)
OV
Vcc
VM
OV
BLa
BLb
(NON-USE)
OV
FLOATING
OV
SG1
OV
Vcc
VM
OV
CG2
OV
Vcc
VM
VPP
OV
CG1,3-8
OV
Vcc
VM
OV
φPa
OV
Vcc
VM
OV
φPb
OV
Vcc
VM
OV
φRa
Vcc
OV
Vcc
φRb
Vcc
OV
Vcc
φFa
OV
Vcc
VM
OV
φFb
OV
I/O
DON'T CARE
DON'T CARE
DATA
LOAD
CYCLE
PRE-CHARGE
CYCLE

FIG. 37

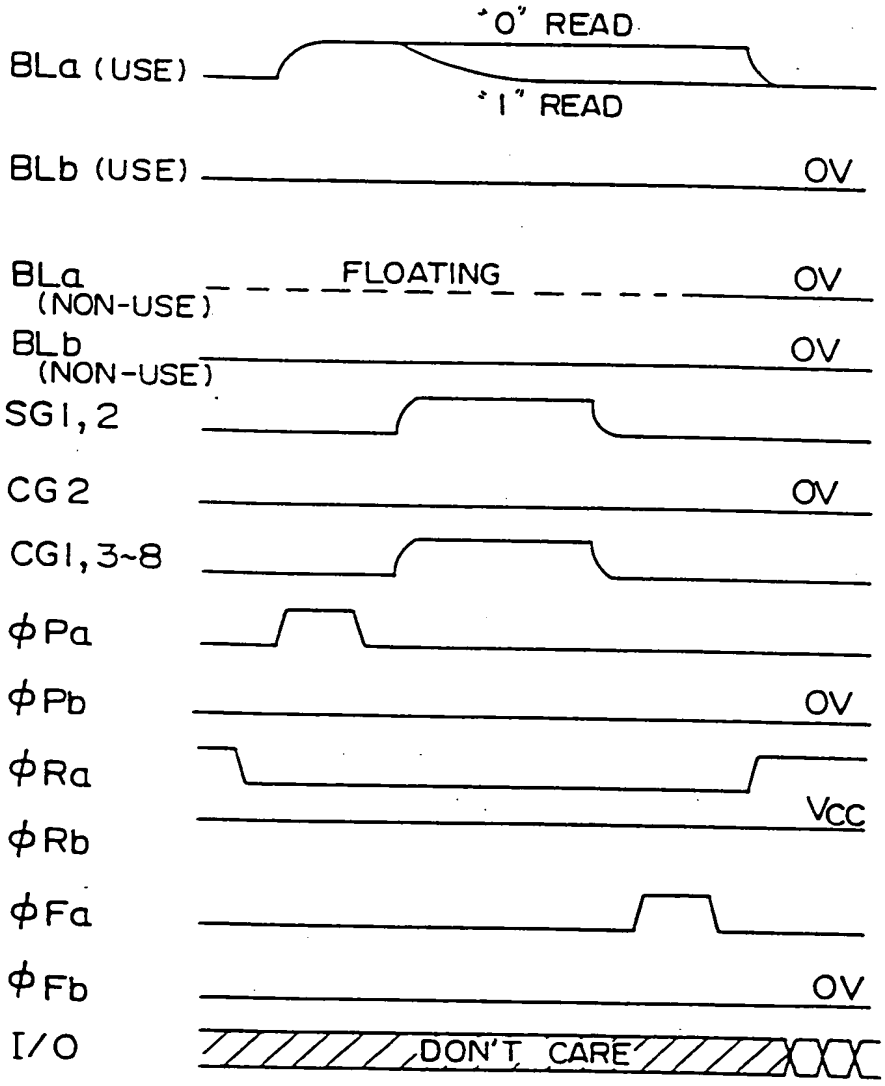

"0" READ
BLa (USE)
"1" READ
BLb (USE)
0V
BLa (NON-USE)
FLOATING
0V
BLb (NON-USE)
0V
SG1, 2
CG2
0V
CG1, 3~8
φPa
φPb
0V
φRa
Vcc
φRb
φFa
φFb
0V
I/O
DON'T CARE

FIG. 38

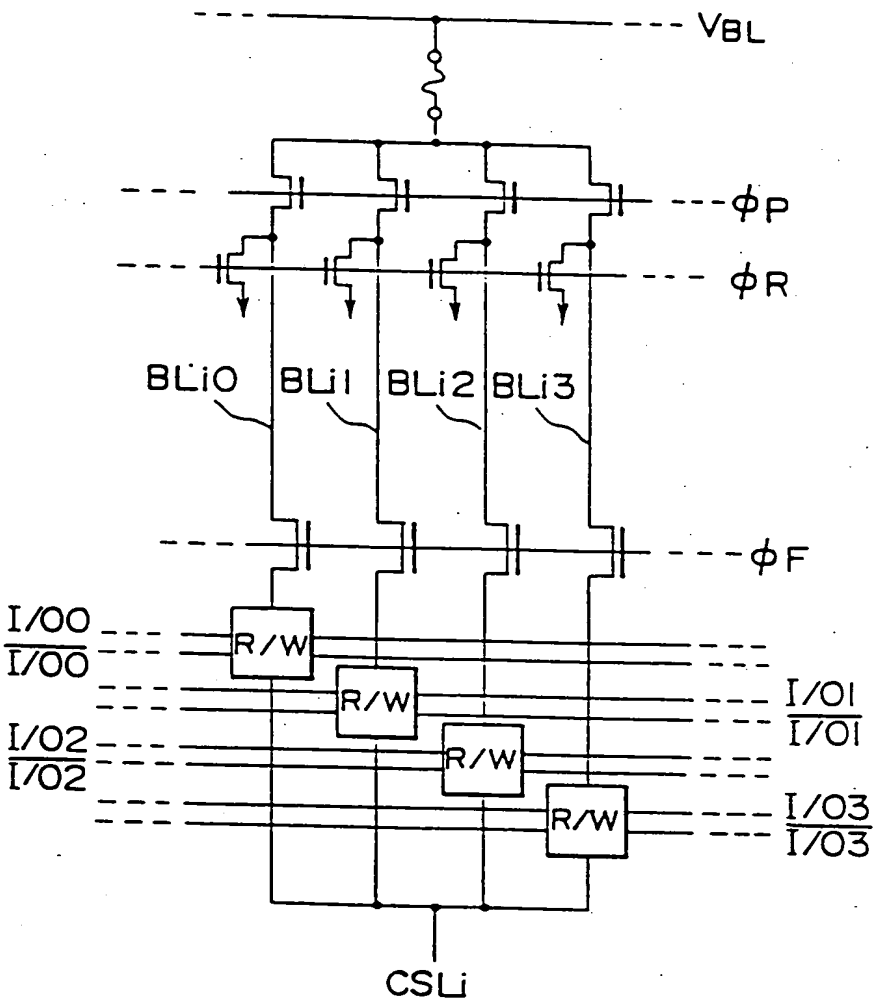

VBL
φP
φR
BLi0
BLi1
BLi2
BLi3
φF
I/00
I/00
R/W
R/W
R/W
R/W
I/01
I/01
I/02
I/02
I/03
I/03
CSLi

FIG.39

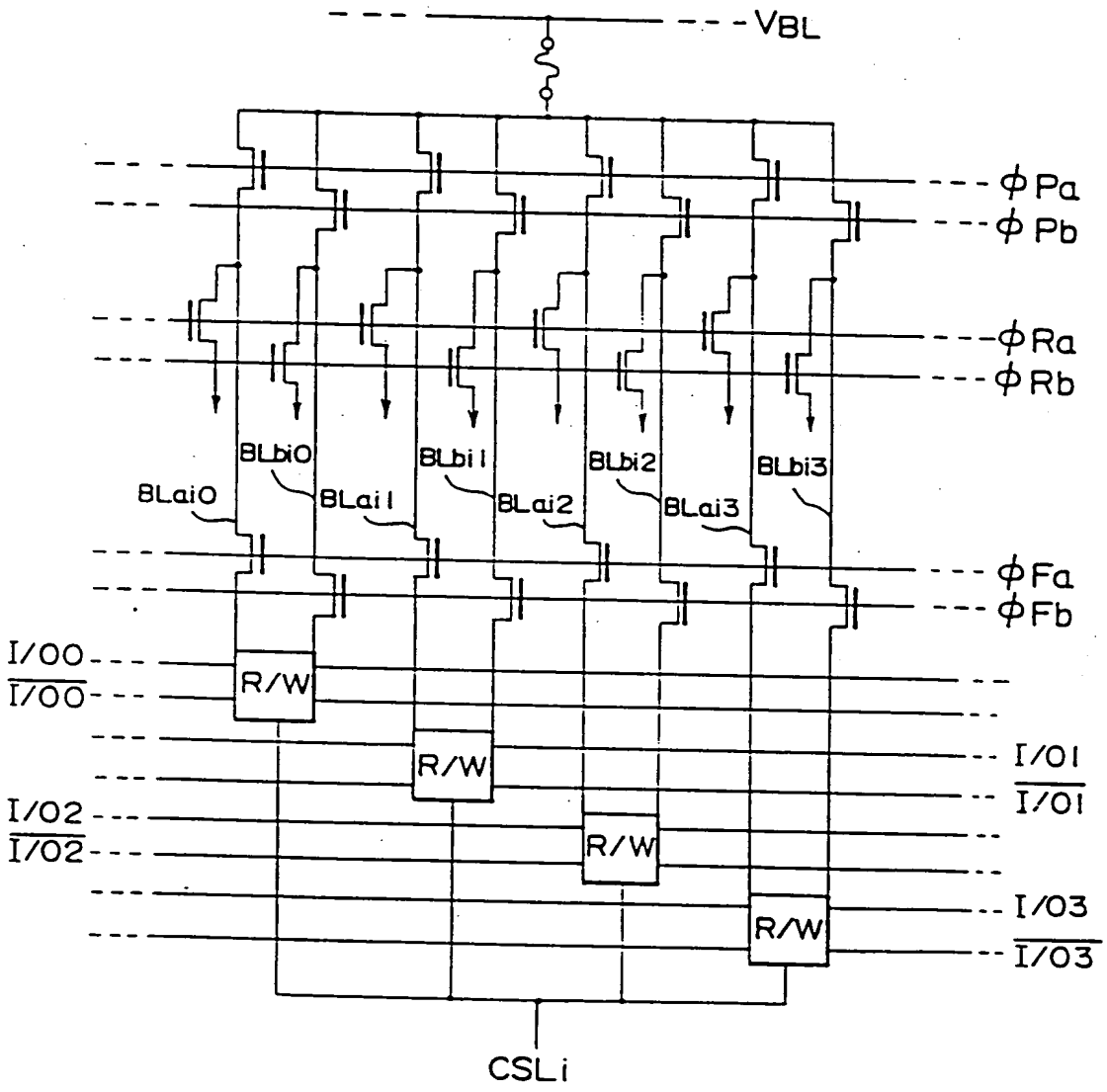

VBL
φPa
φPb
φRa
φRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
R/W
R/W
R/W
R/W
I/01
I/01
I/02
I/02
I/03
I/03
CSLi

FIG. 40

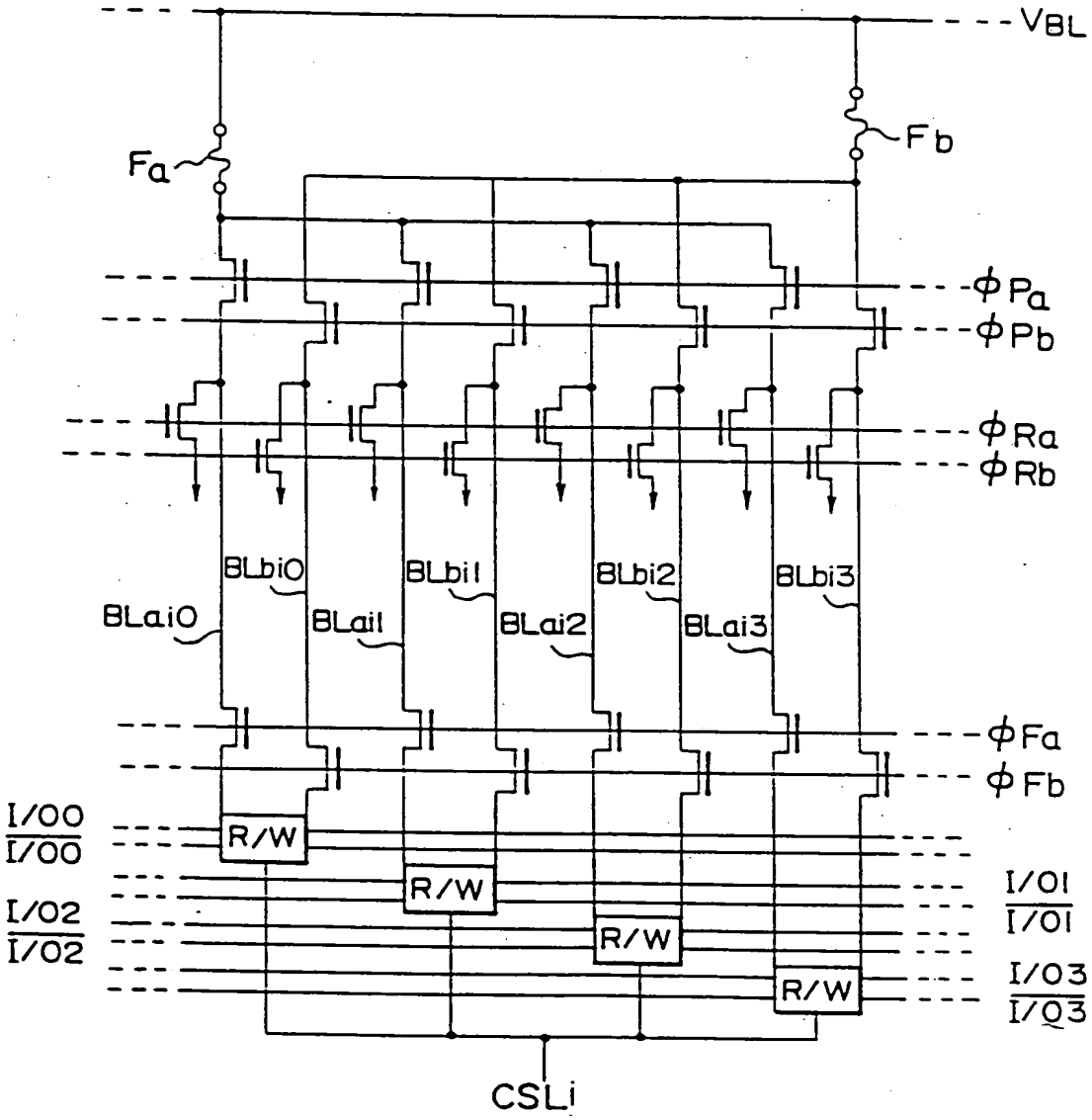

VBL
Fa
Fb
φPa
φPb
φRa
φRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
R/W
R/W
R/W
R/W
I/02
I/02
I/01
I/01
I/03
I/03
CSLi

FIG. 41

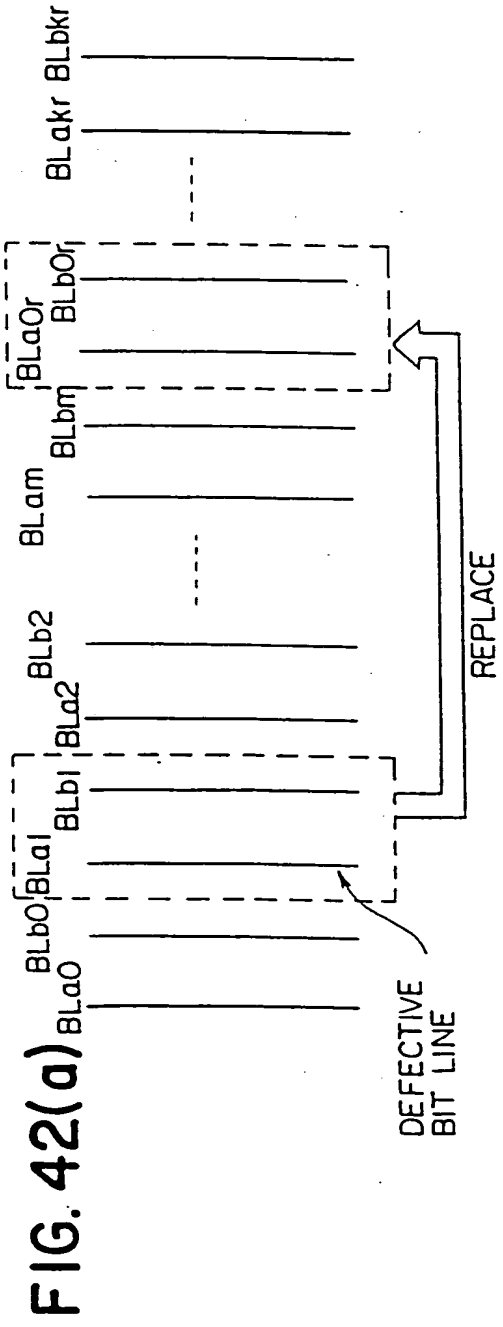


FIG. 42(a)

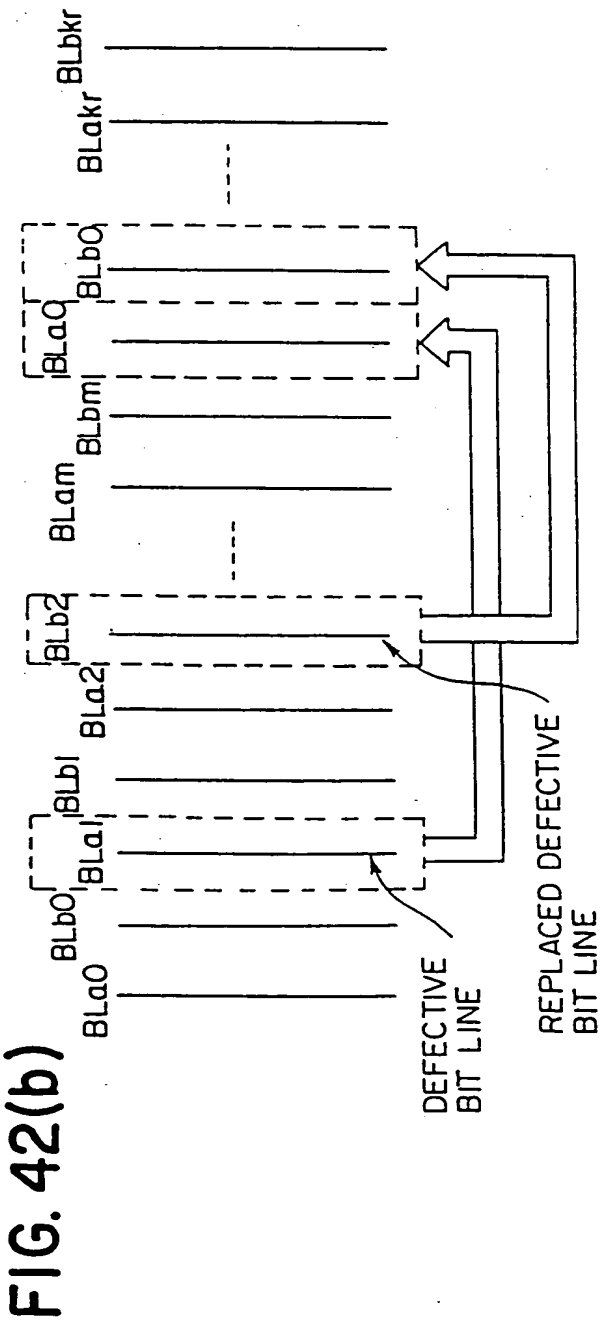


FIG. 42(b)

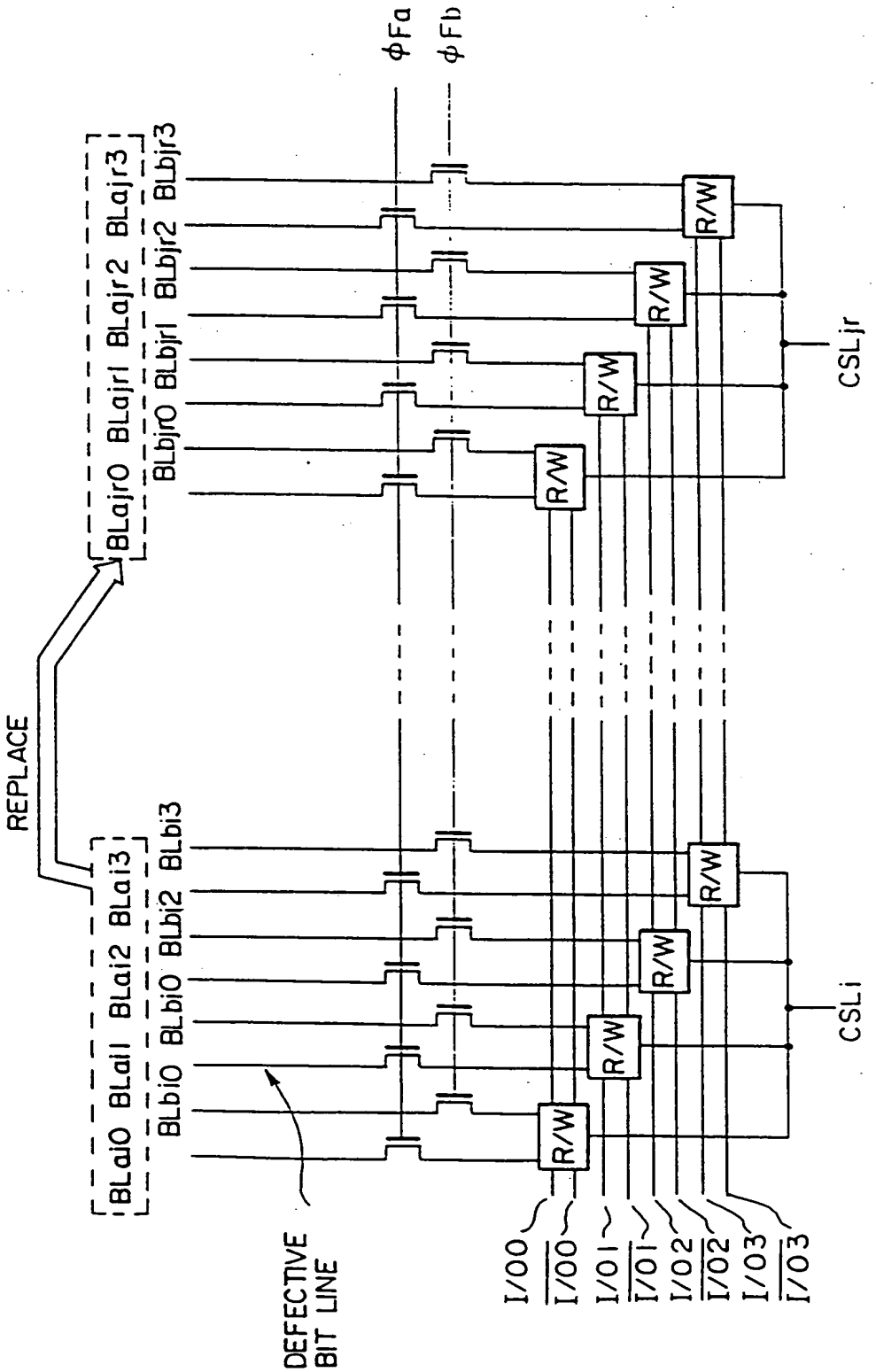

φFa
φFb
BLajr3 BLajr2 BLajr1 BLajr0 BLbjr3 BLbjr2 BLbjr1 BLbjr0
REPLACE
BLai3 BLai2 BLai1 BLai0 BLbi3 BLbi2 BLbi1 BLbi0
R/W
CSLjr
CSLi
DEFECTIVE BIT LINE
I/O0 I/O0 I/O1 I/O1 I/O2 I/O2 I/O3 I/O3

FIG. 43

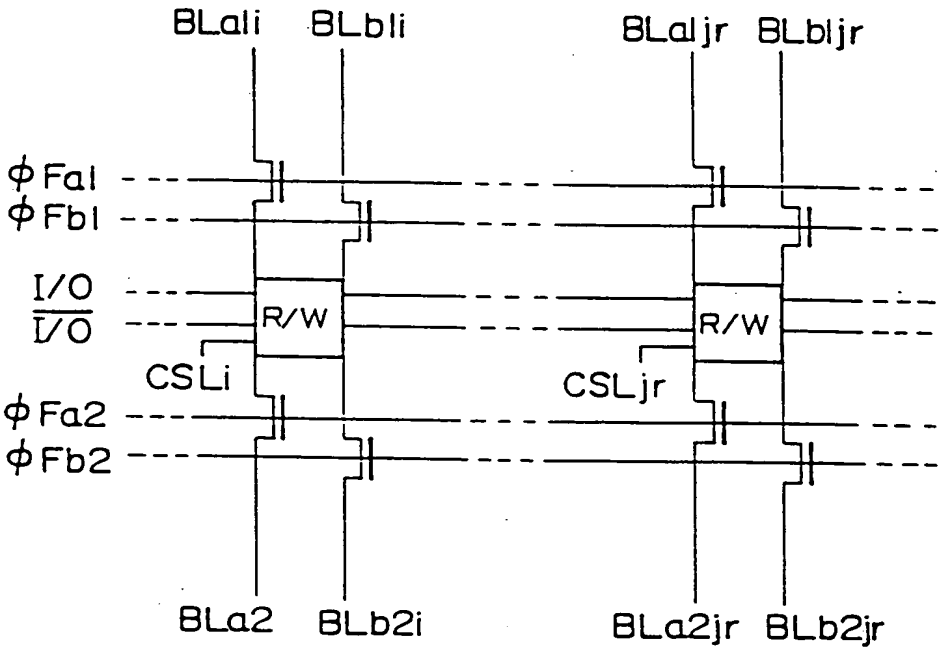

BLali
BLbli
BLaljr
BLbljr
φFal
φFbl
I/O
I/O
R/W
R/W
CSLi
CSLjr
φFa2
φFb2
BLa2
BLb2i
BLa2jr
BLb2jr

FIG.44

FIG. 45(a)

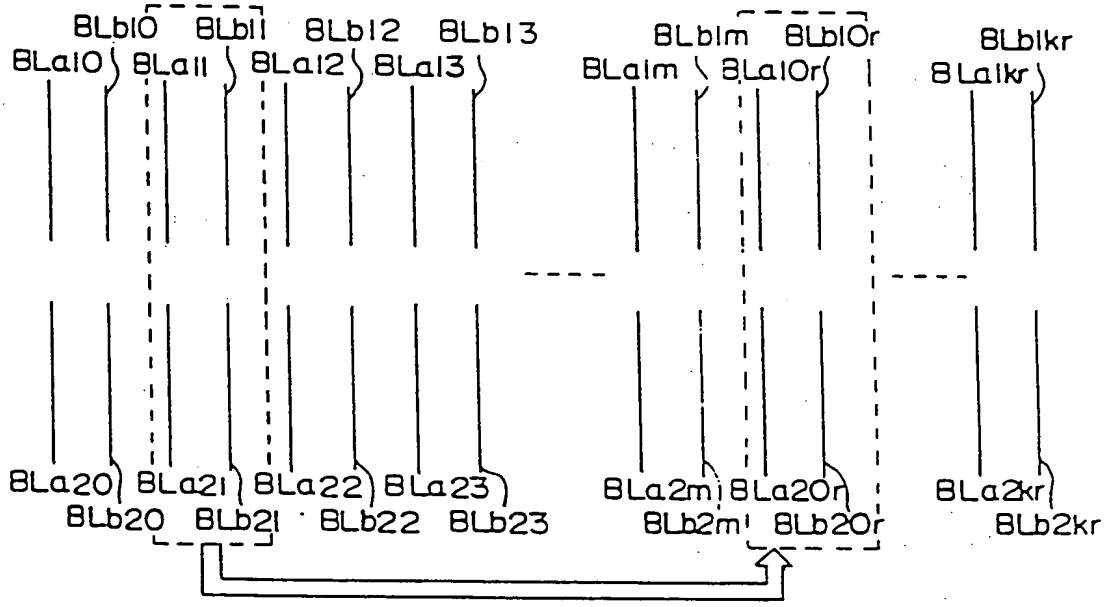


FIG. 45(b)

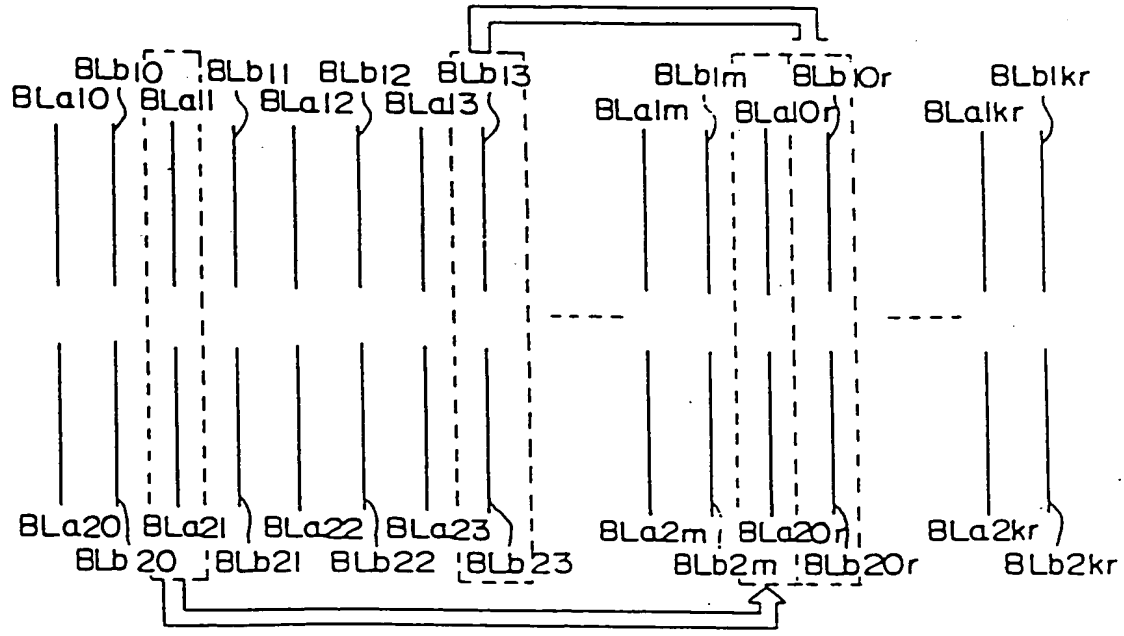


FIG. 46(a)

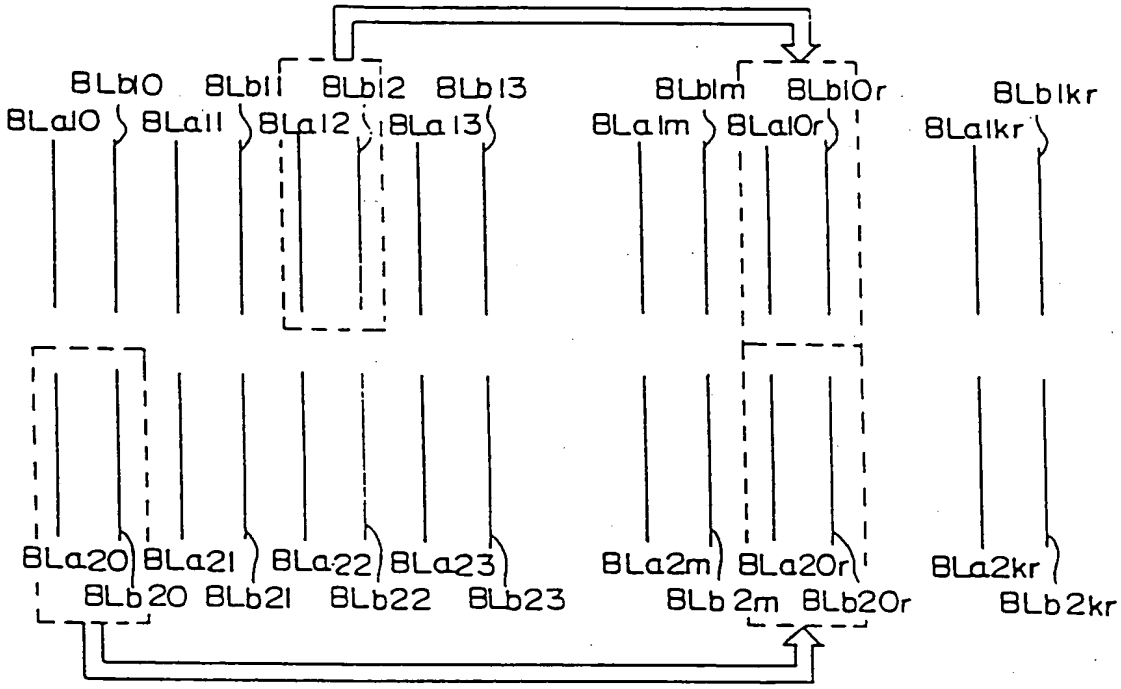
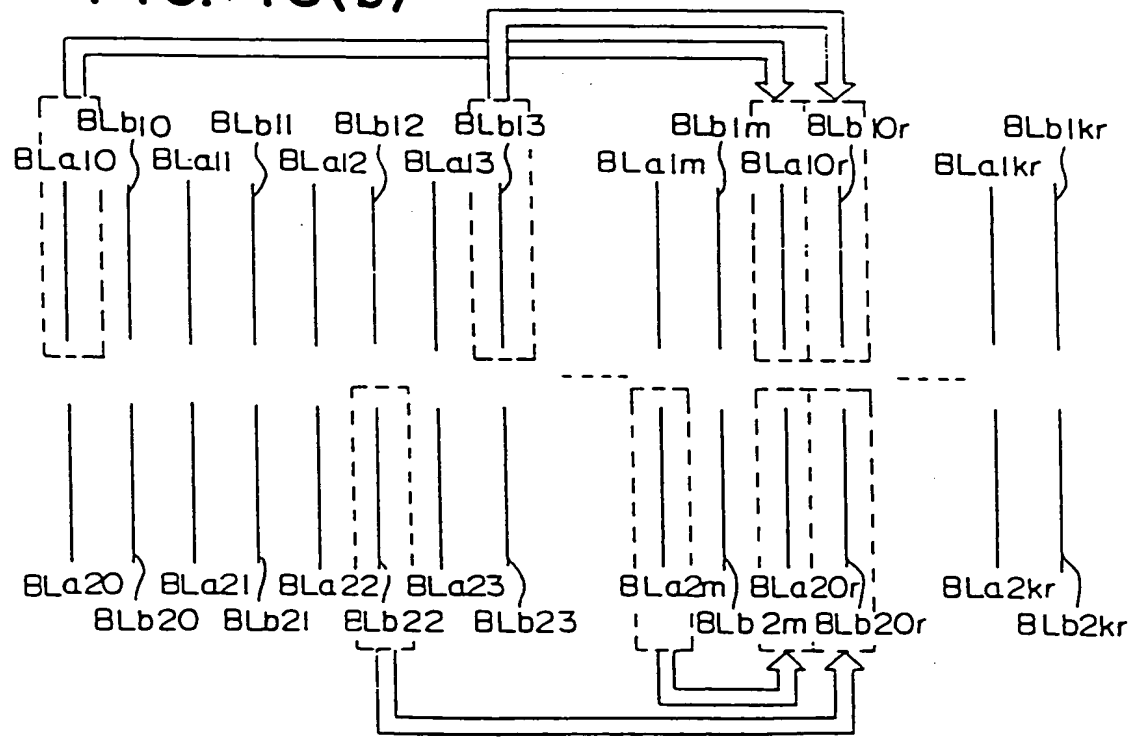


FIG. 46(b)



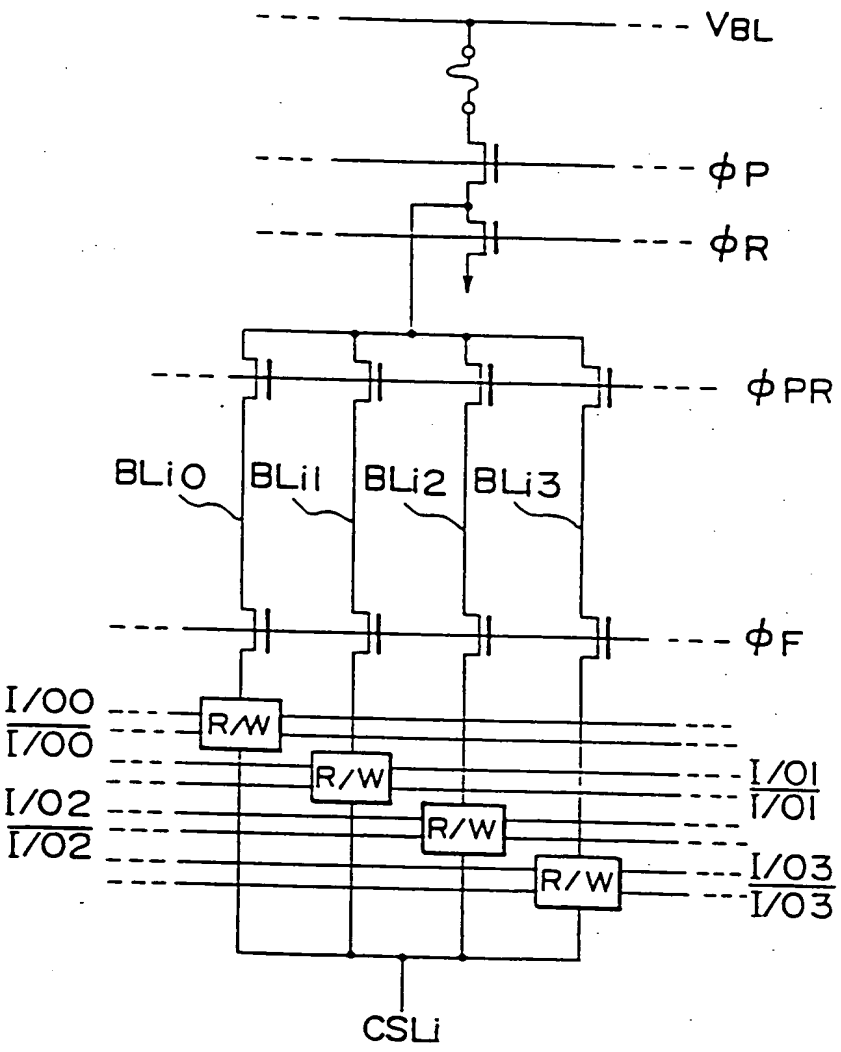

VBL
φP
φR
φPR
BLi0
BLi1
BLi2
BLi3
φF
I/O0
I/O0
I/O2
I/O2
R/W
R/W
R/W
R/W
I/O1
I/O1
I/O3
I/O3
CSLi

FIG. 47

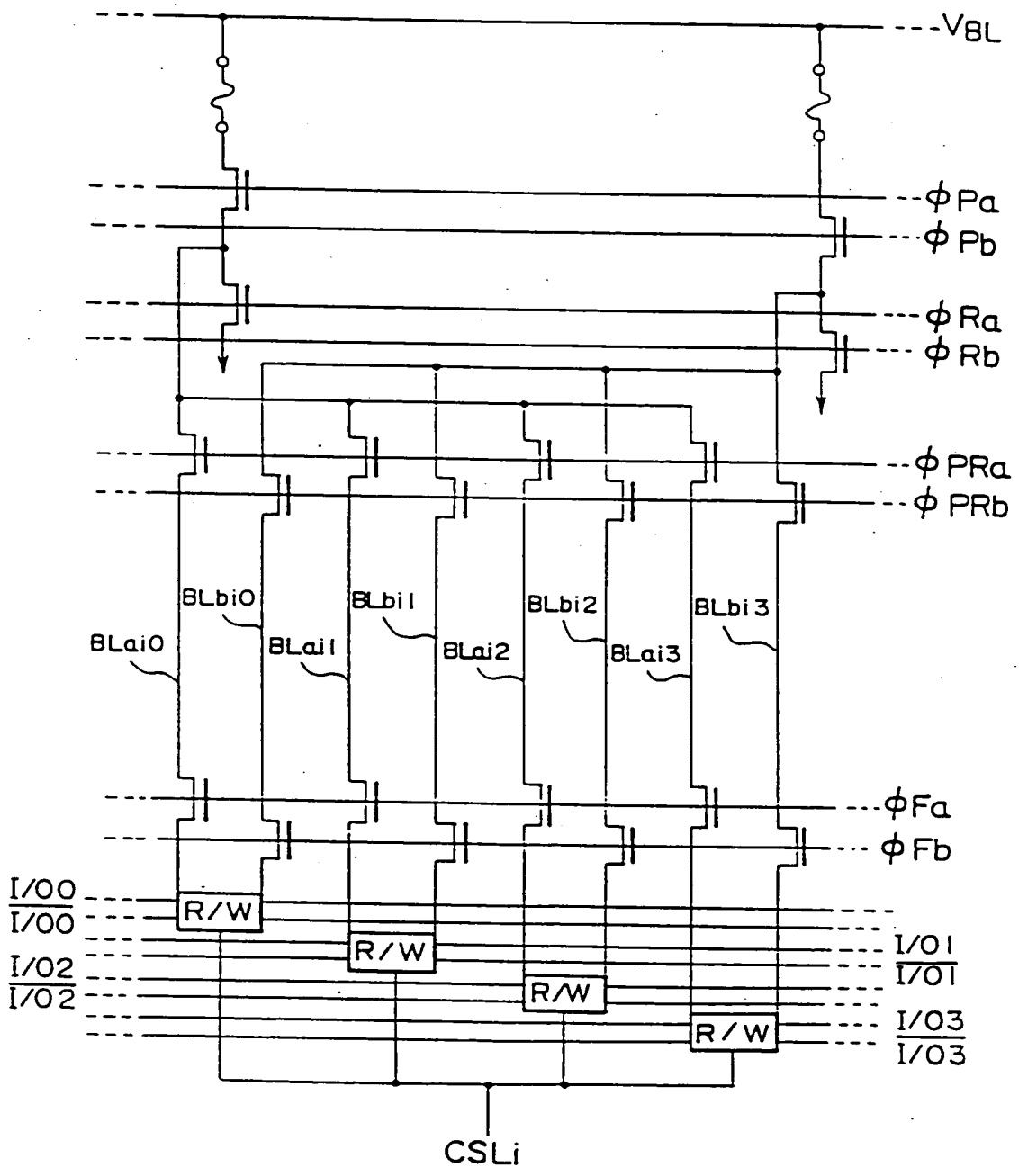

VBL
φPa
φPb
φRa
φRb
φPRa
φPRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/00
I/00
I/02
I/02
R/W
R/W
R/W
R/W
I/01
I/01
I/03
I/03
CSLi

FIG. 48

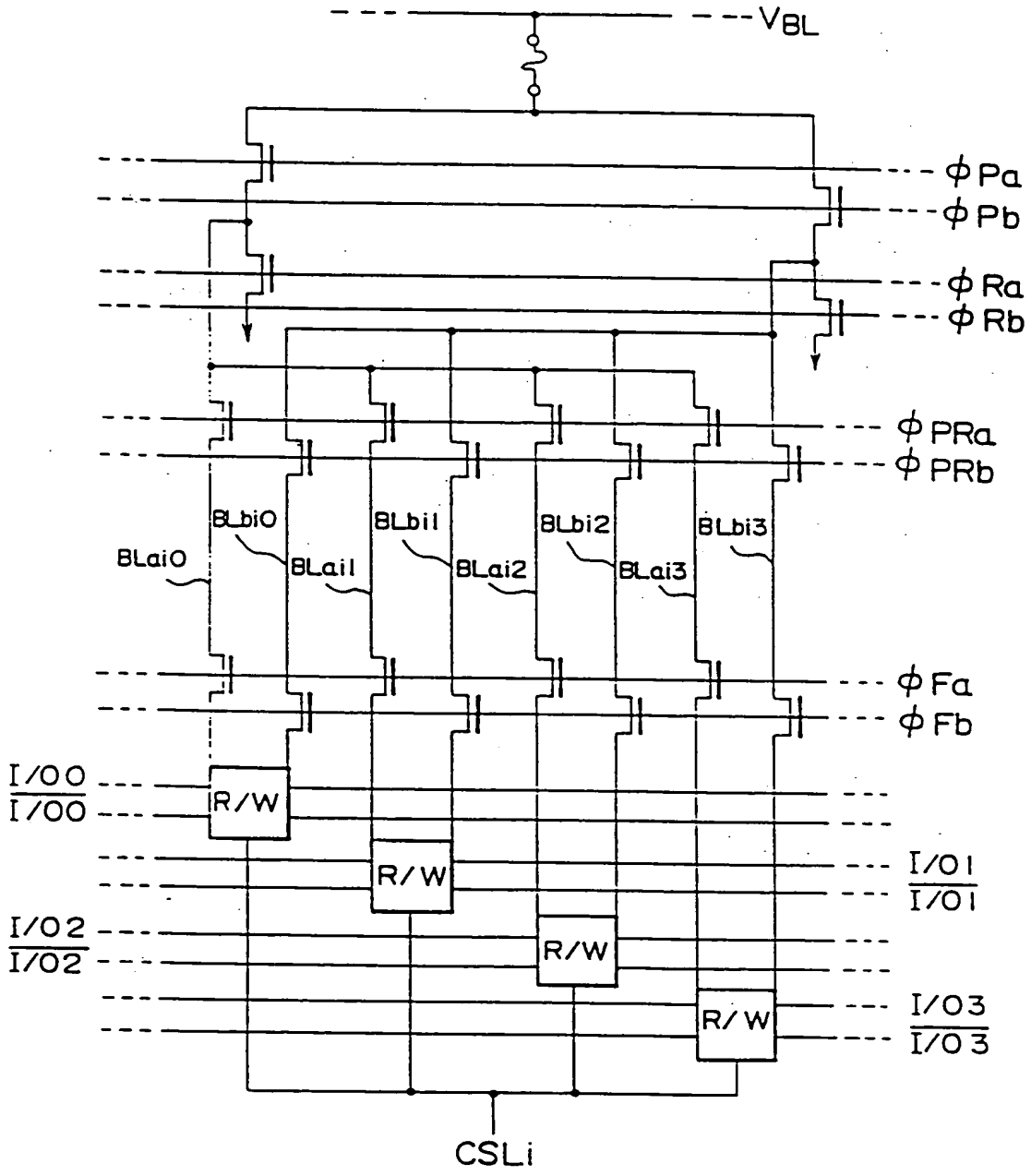

VBL
φPa
φPb
φRa
φRb
φPRa
φPRb
BLbi0
BLbi1
BLbi2
BLbi3
BLai0
BLai1
BLai2
BLai3
φFa
φFb
I/O0
I/O0
R/W
R/W
R/W
R/W
I/O1
I/O1
I/O2
I/O2
I/O3
I/O3
CSLi

FIG. 49

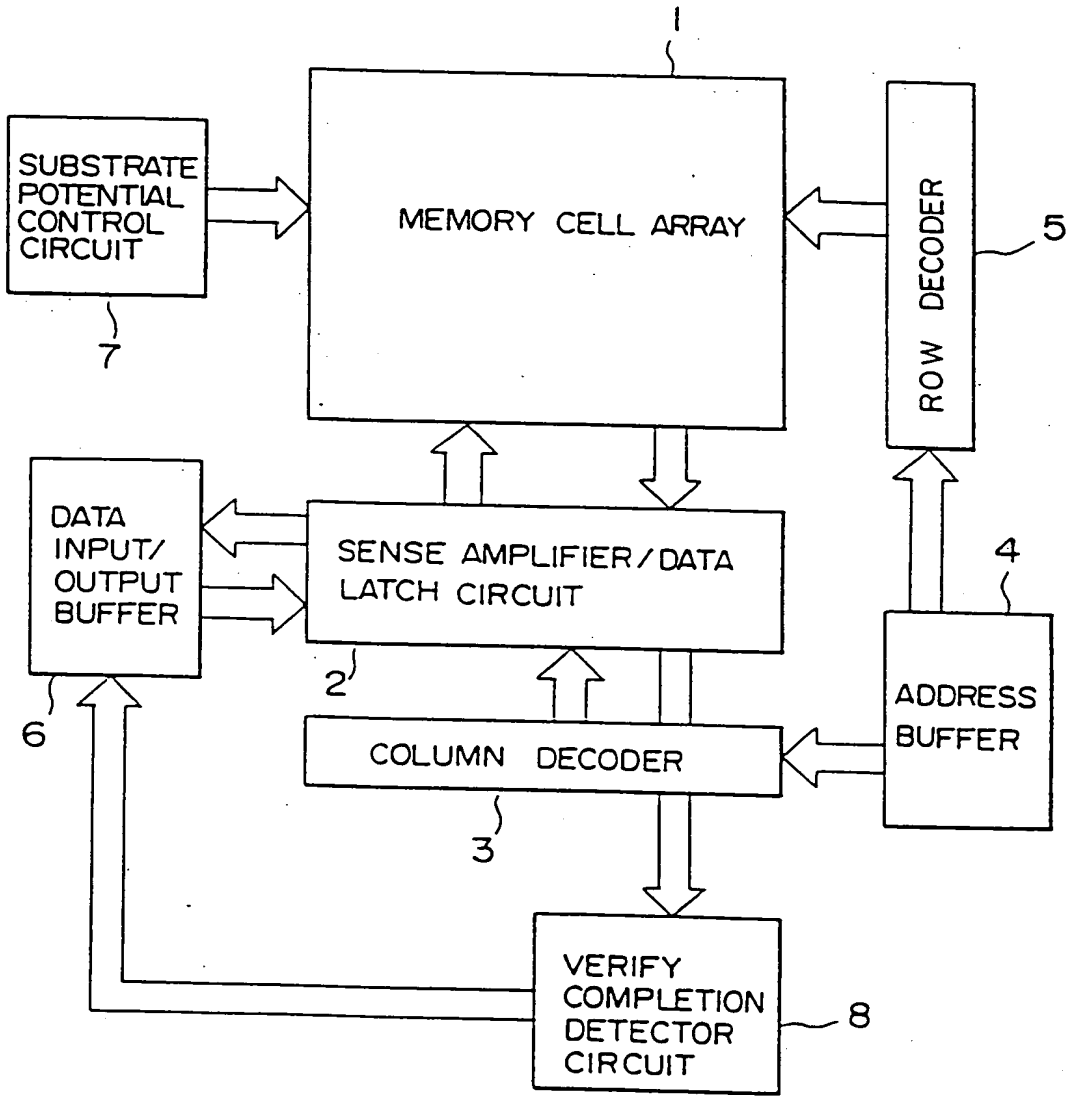

1
SUBSTRATE POTENTIAL CONTROL CIRCUIT
7
MEMORY CELL ARRAY
ROW DECODER
5
DATA INPUT/ OUTPUT BUFFER
6
SENSE AMPLIFIER/DATA LATCH CIRCUIT
2
4
ADDRESS BUFFER
COLUMN DECODER
3
VERIFY COMPLETION DETECTOR CIRCUIT
8

FIG. 50

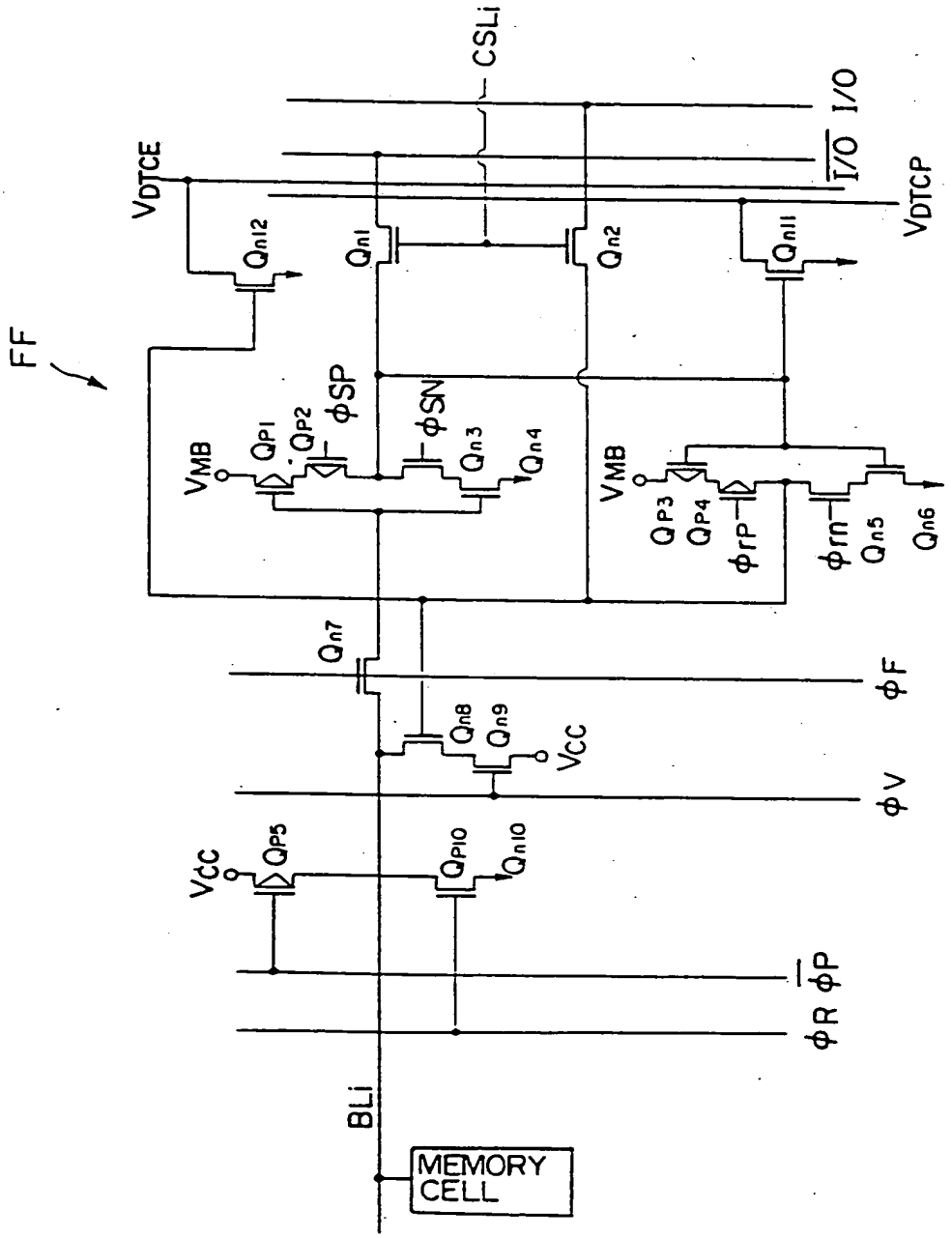

CSLi
I/O
$\overline{I/O}$
VDTCE
VDTCP
Qn12
Qn1
Qn2
Qn11
FF
φSP
φSN
VMB
QP1
QP2
Qn3
Qn4
VMB
QP3
QP4
φrP
φrn
Qn5
Qn6
Qn7
φF
Qn8
Qn9
VCC
φV
VCC
QP5
QP10
Qn10
$\overline{\phi R}$ φP
BLi
MEMORY CELL

FIG. 51

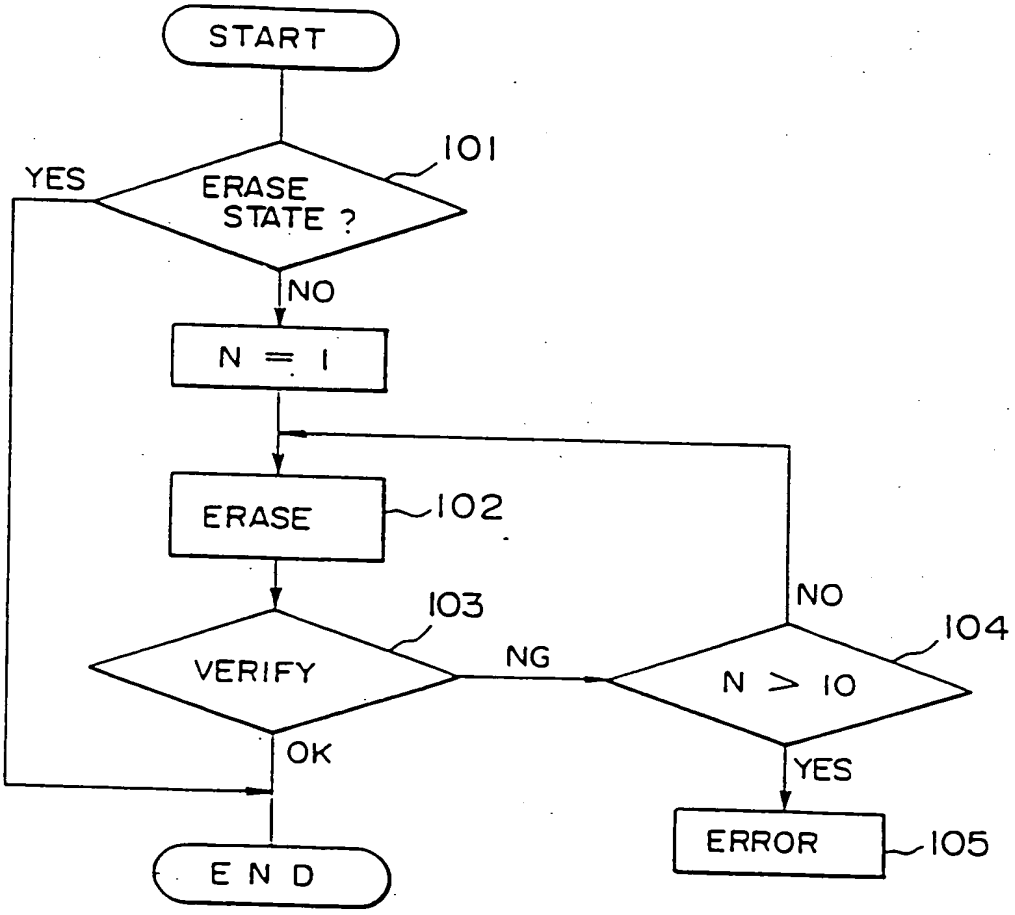

START
ERASE STATE ?
101
YES
NO
N = 1
ERASE
102
VERIFY
103
NG
OK
N > 10
104
NO
YES
ERROR
105
E N D

FIG. 52

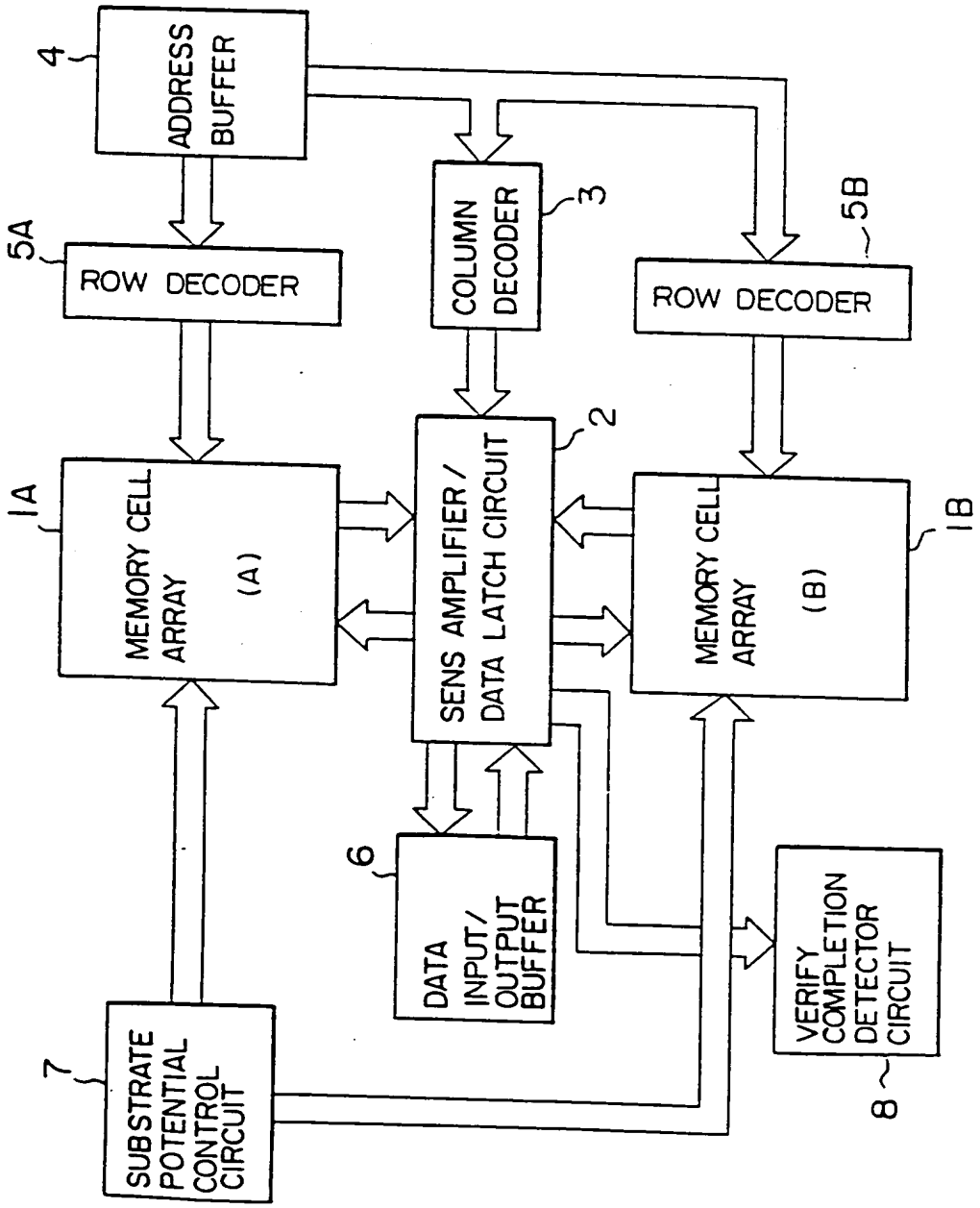

4
ADDRESS BUFFER
5A
ROW DECODER
COLUMN DECODER
3
5B
ROW DECODER
1A
MEMORY CELL ARRAY (A)
SENS AMPLIFIER / DATA LATCH CIRCUIT
2
MEMORY CELL ARRAY (B)
1B
6
DATA INPUT/ OUTPUT BUFFER
VERIFY COMPLETION DETECTOR CIRCUIT
8
7
SUBSTRATE POTENTIAL CONTROL CIRCUIT

FIG. 53

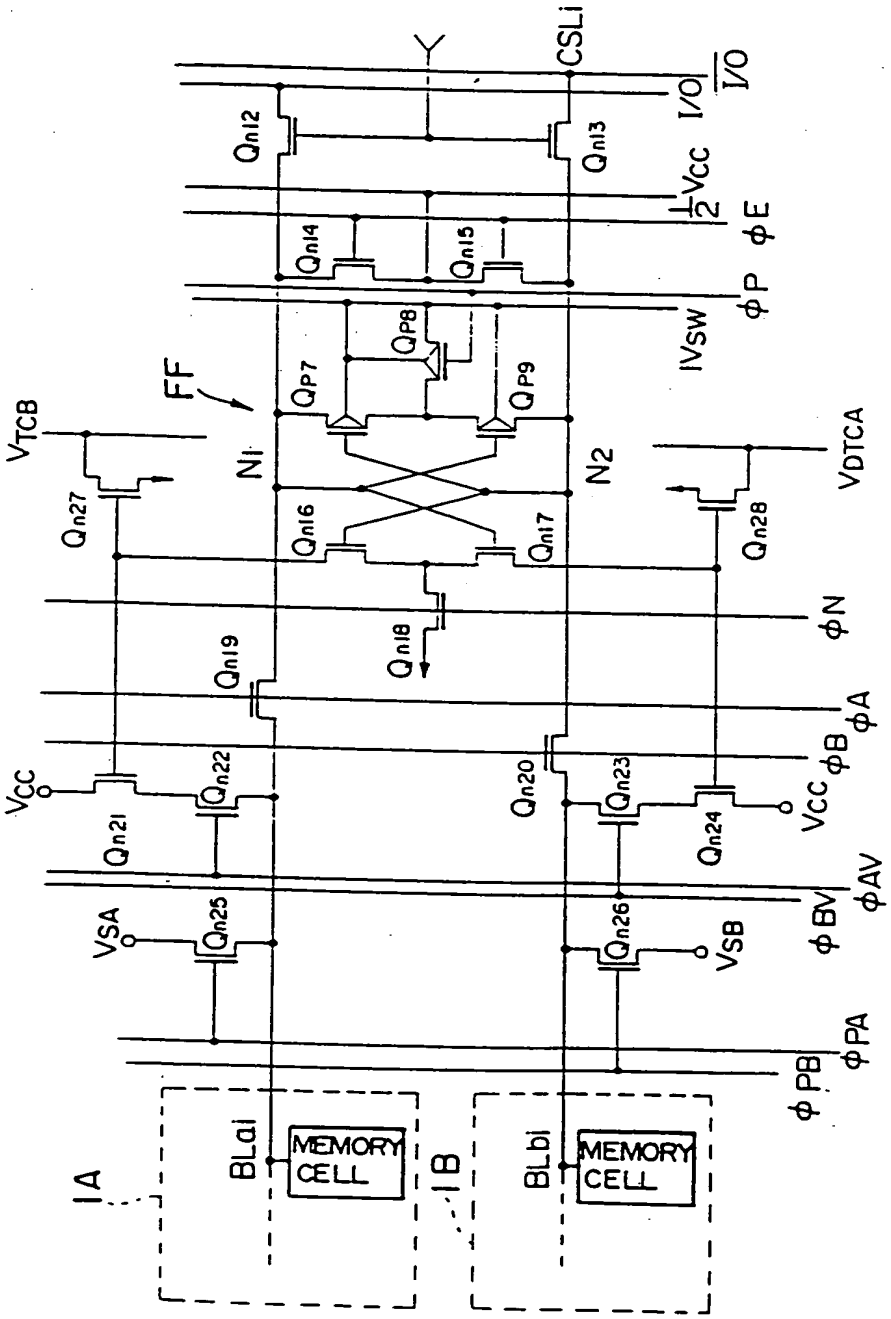

Y
CSLi
I/O
$\overline{I/O}$
Qni2
Qni3
$\frac{1}{2}$Vcc
φE
Qni4
Qni5
φP
IVSW
QP8
FF
QP7
QP9
VTCB
Ni
N2
VDTCA
Qn27
Qni6
Qni7
Qn28
φN
Qni8
Qni9
φA
φB
Vcc
Qn22
Qn20
Qn23
Vcc
Qn21
Qn24
φAV
φBV
VSA
Qn25
Qn26
VSB
φPA
φPB
BLai
MEMORY CELL
BLbi
MEMORY CELL
IA
IB

FIG. 54

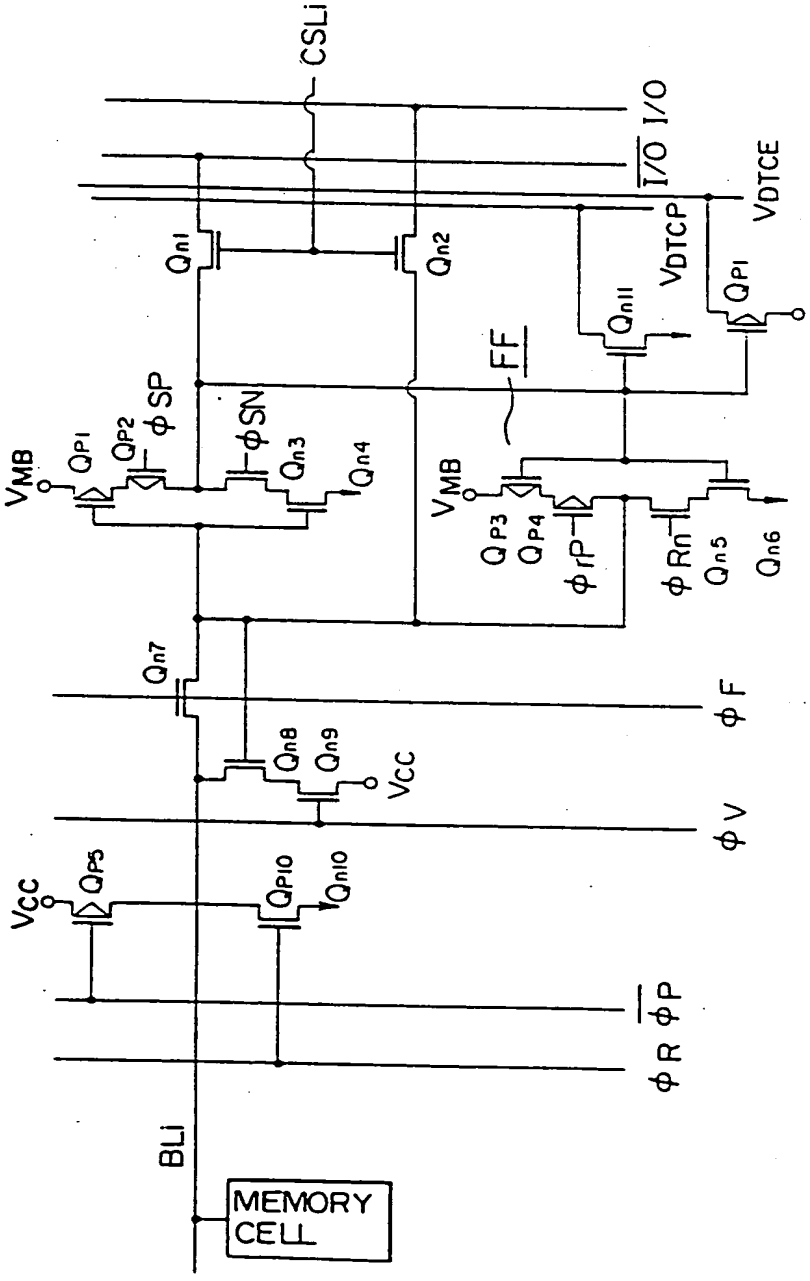

CSLi
I/O
VDTCE
VDTCP
Qn1
Qn2
QP1
Qn11
FF
VMB
QP1
QP2
φSP
φSN
Qn3
Qn4
VMB
QP3
QP4
φrP
φRn
Qn5
Qn6
Qn7
φF
Qn8
Qn9
VCC
φV
VCC
QP5
QP10
Qn10
φRφP
BLi
MEMORY CELL

FIG.55

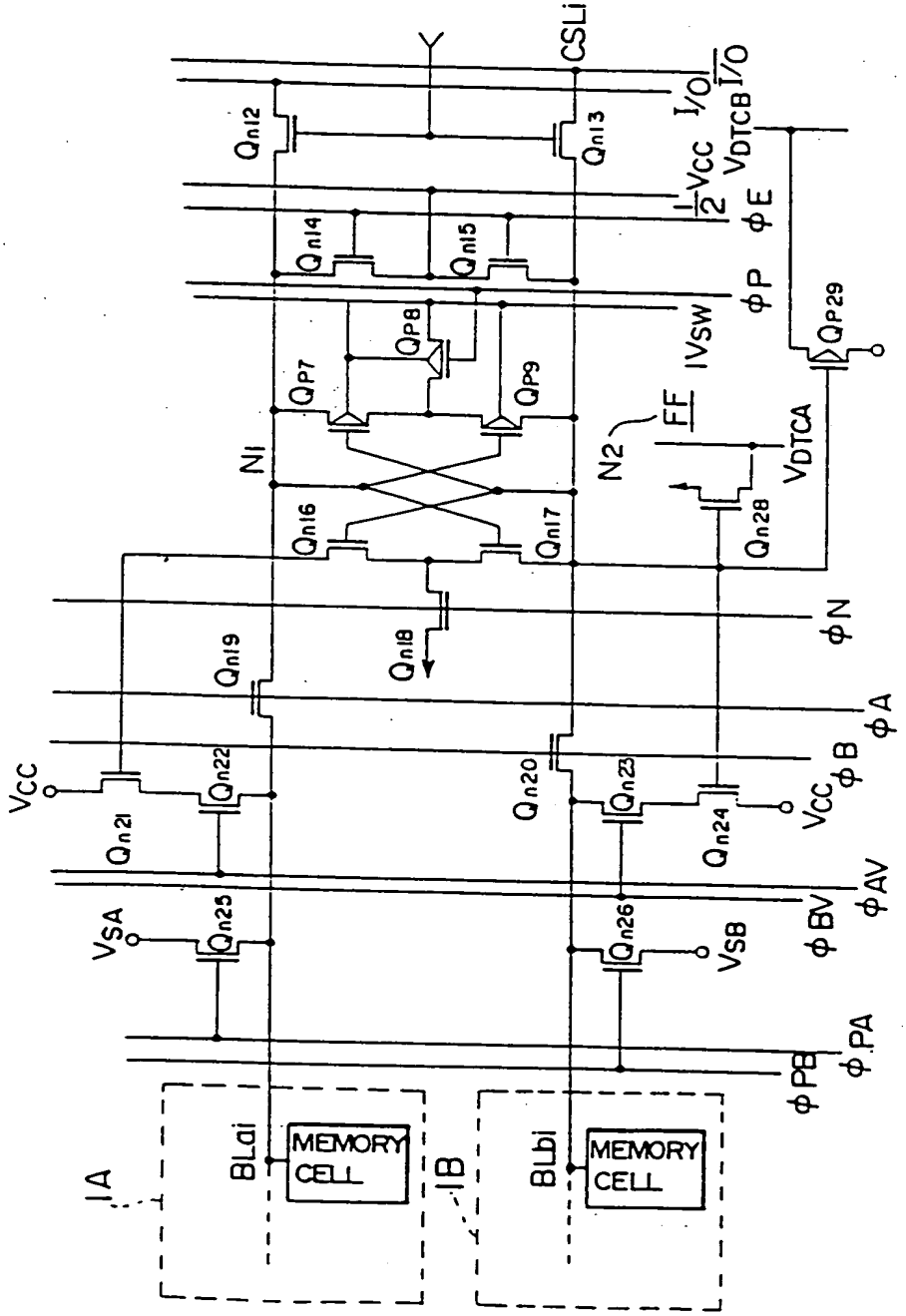

Y
CSLi
I/O
I/O
Qn12
Qn13
VDTCB
1/2 Vcc
φE
Qn14
Qn15
φP
IVSW
QP29
QP8
QP7
QP9
FF
N2
VDTCA
N1
Qn16
Qn17
Qn28
φN
Qn18
Qn19
φA
Vcc
Qn22
Qn20
Qn23
φB
Vcc
Qn21
Qn24
φAV
φBV
VSA
Qn25
Qn26
VSB
φPA
φPB
BLai
MEMORY CELL
BLbi
MEMORY CELL
IA
IB

FIG. 56

FIG. 57(a)

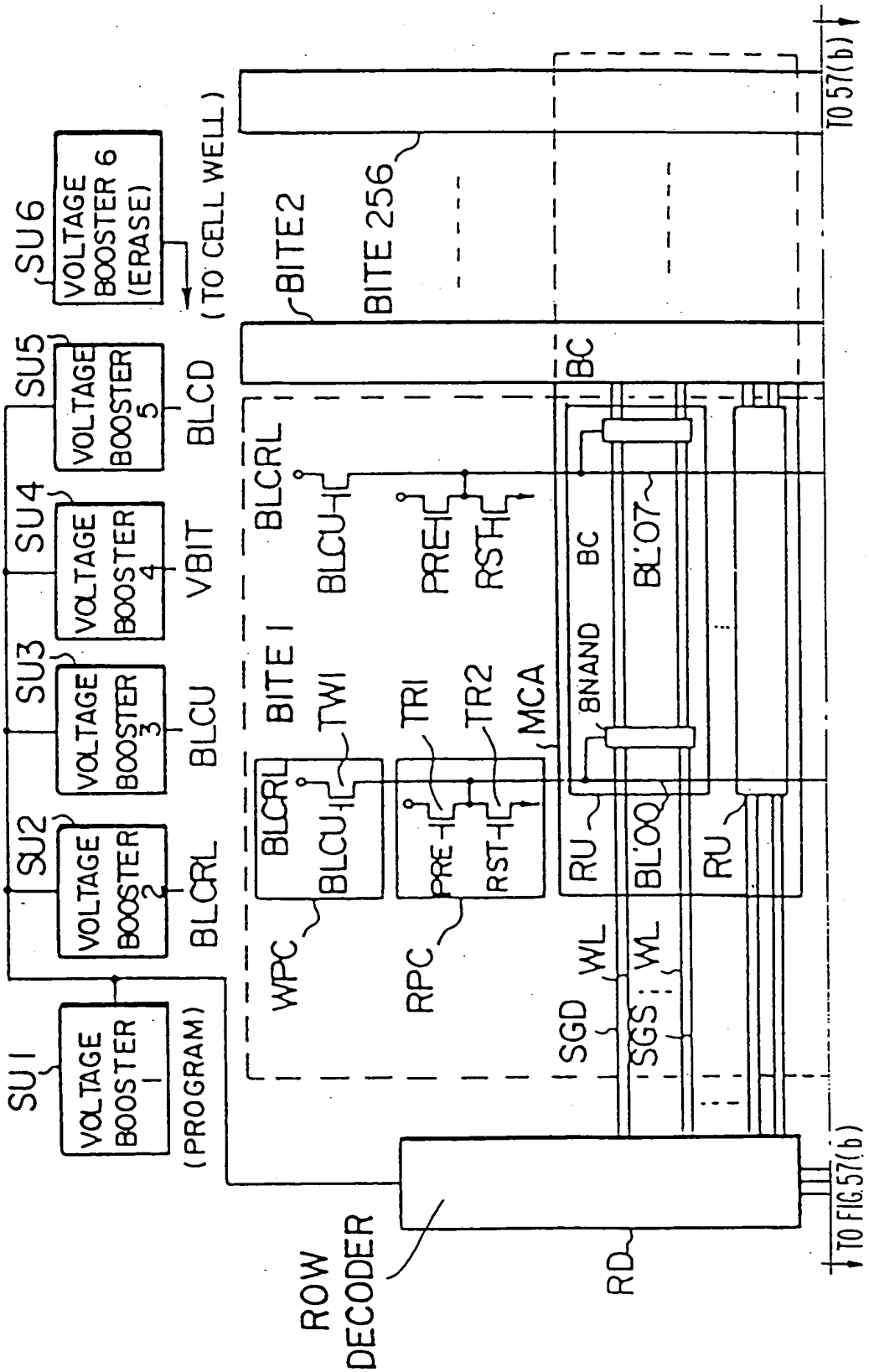

SU1
VOLTAGE BOOSTER 1
(PROGRAM)
SU2
VOLTAGE BOOSTER 2
BLCRL
SU3
VOLTAGE BOOSTER 3
BLCU
SU4
VOLTAGE BOOSTER 4
VBIT
SU5
VOLTAGE BOOSTER 5
BLCD
SU6
VOLTAGE BOOSTER 6 (ERASE)
(TO CELL WELL)
BITE1
BITE2
BITE 256
BC
BLCRL
BLCU
TWI
TRI
TR2
MCA
PRE
RST
WPC
RPC
SGD
WL
SGS
8NAND
RU
BL'00
BL'07
ROW DECODER
RD
TO 57(b)
TO FIG.57(b)

FIG. 57(b)

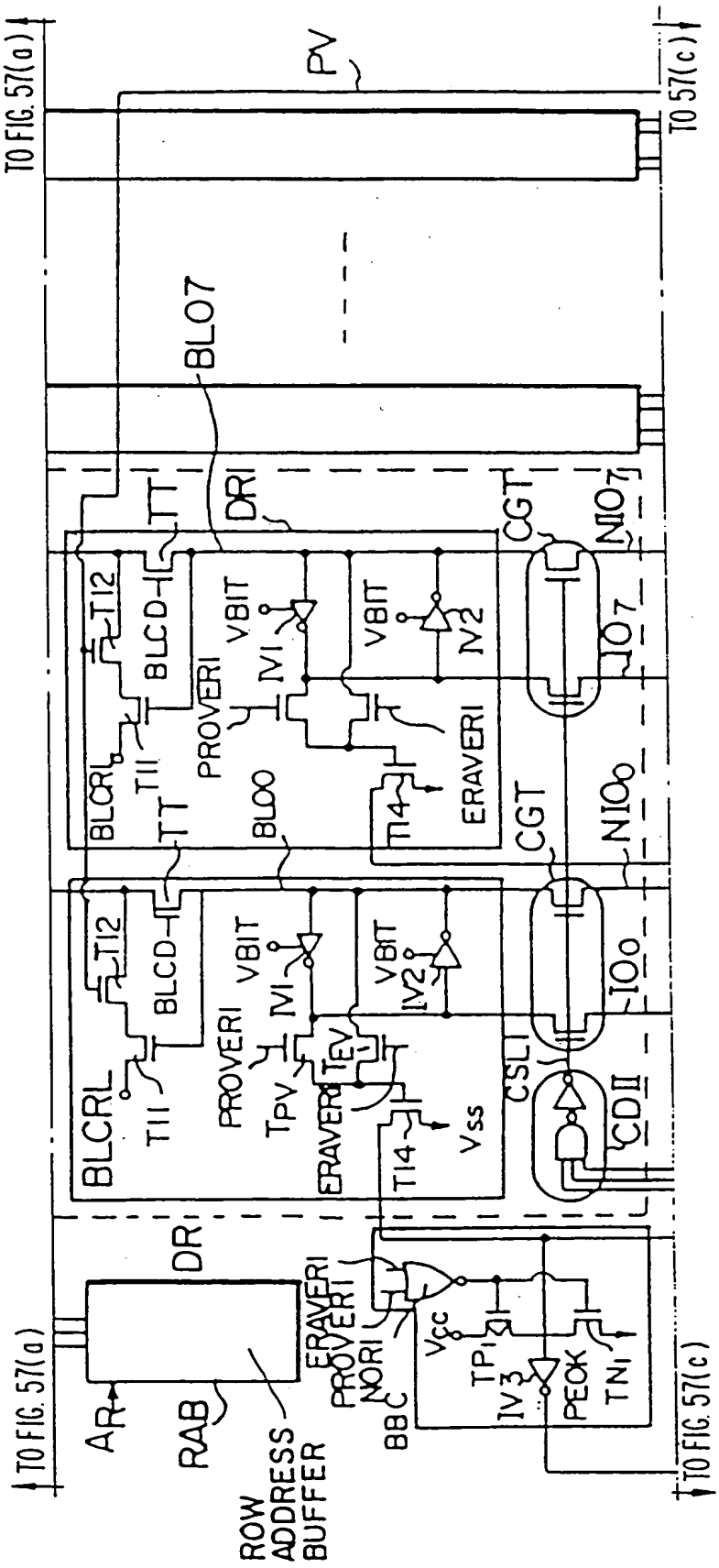
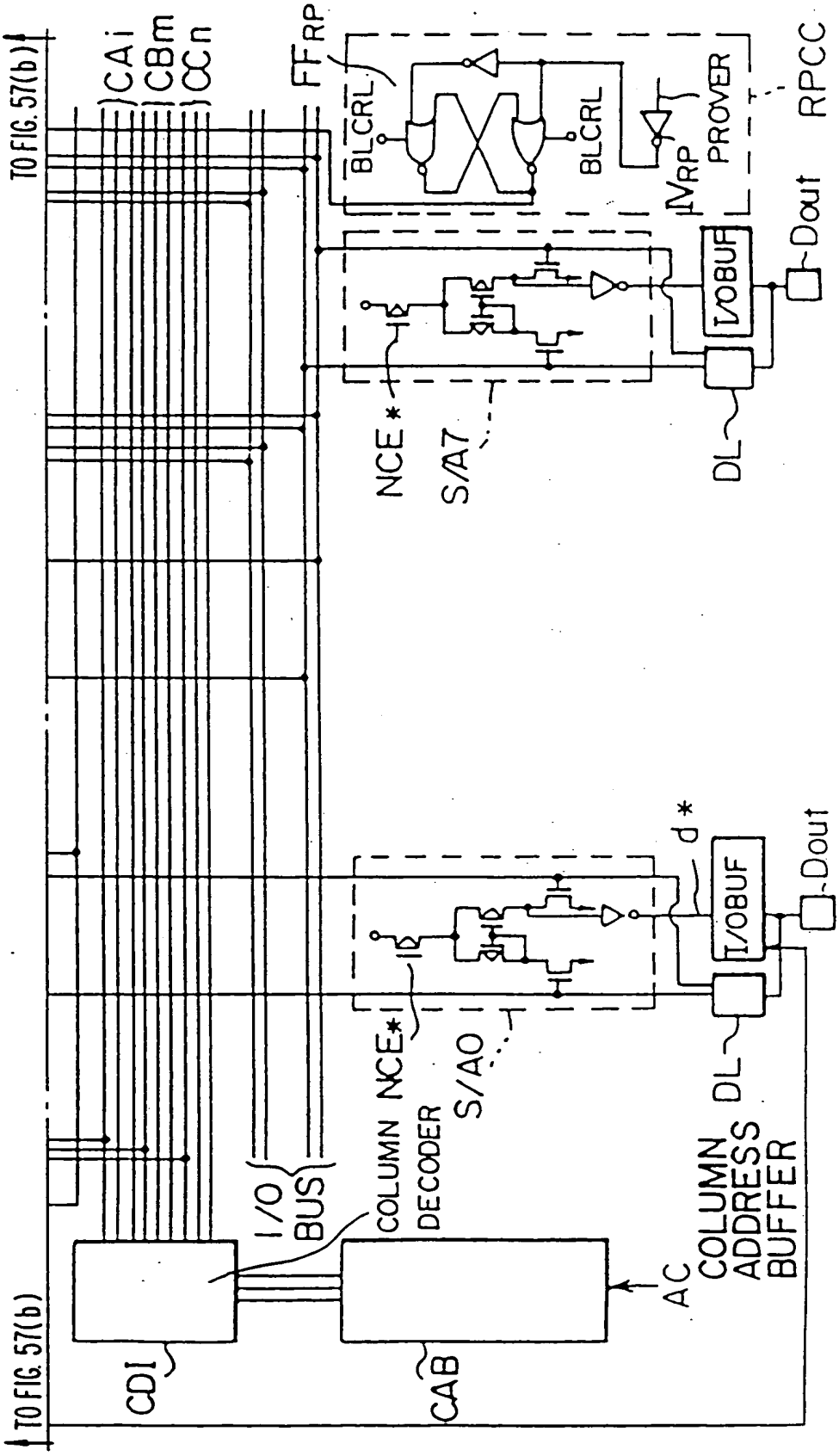

TO FIG. 57(a)
TO 57(c)
PV
BL07
DRI
TT
CGT
NIO7
IO7
T12
BLCD
VBIT
IV1
IV2
PROVERI
ERAVERI
T11
T14
BLCRL
BL00
NIO0
IO0
CSL1
CDI1
TPV
TEV
Vss
DR
ERAVERI
PROVERI
NORI
BBC
Vcc
TP1
IV3
PEOK
TN1
AR
RAB
ROW ADDRESS BUFFER
TO FIG. 57(a)
TO FIG. 57(c)

FIG. 57(c)


TO FIG. 57(b)
CAi
CBm
CCn
FFRP
BLCRL
BLCRL
VRP
PROVER
RPCC
I/OBUF
Dout
NCE*
S/A7
DL
d*
I/OBUF
Dout
NCE*
S/A0
DL
COLUMN DECODER
I/O BUS
COLUMN ADDRESS BUFFER
AC
CDI
CAB
TO FIG. 57(b)

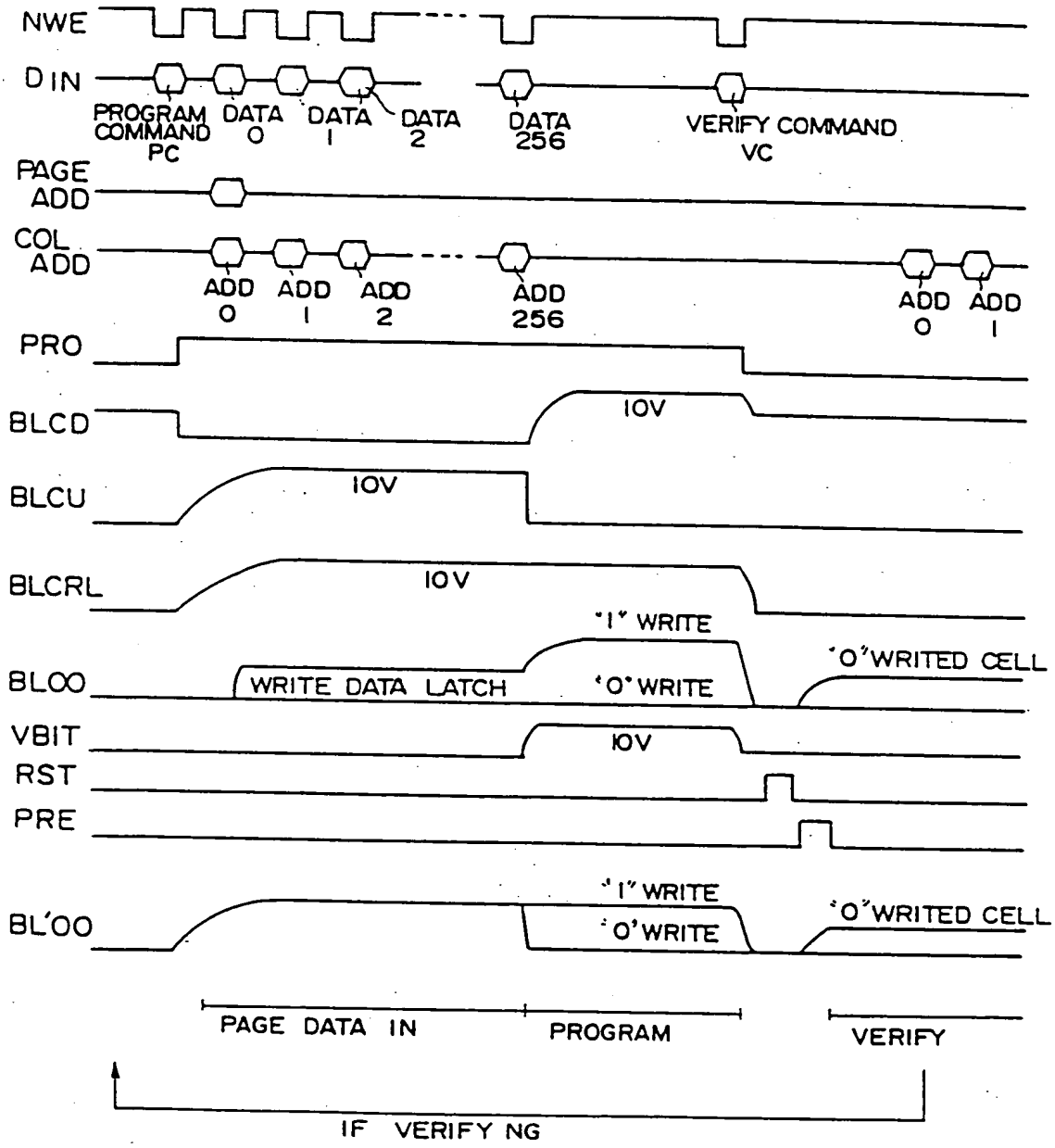

NWE
DIN
PROGRAM COMMAND PC
DATA 0
DATA 1
DATA 2
DATA 256
VERIFY COMMAND VC
PAGE ADD
COL ADD
ADD 0
ADD 1
ADD 2
ADD 256
ADD 0
ADD 1
PRO
BLCD
10V
BLCU
10V
BLCRL
10V
"1" WRITE
"0" WRITED CELL
BLOO
WRITE DATA LATCH
"0" WRITE
VBIT
10V
RST
PRE
"1" WRITE
"0" WRITE
"0" WRITED CELL
BL'OO
PAGE DATA IN
PROGRAM
VERIFY
IF VERIFY NG

FIG. 58

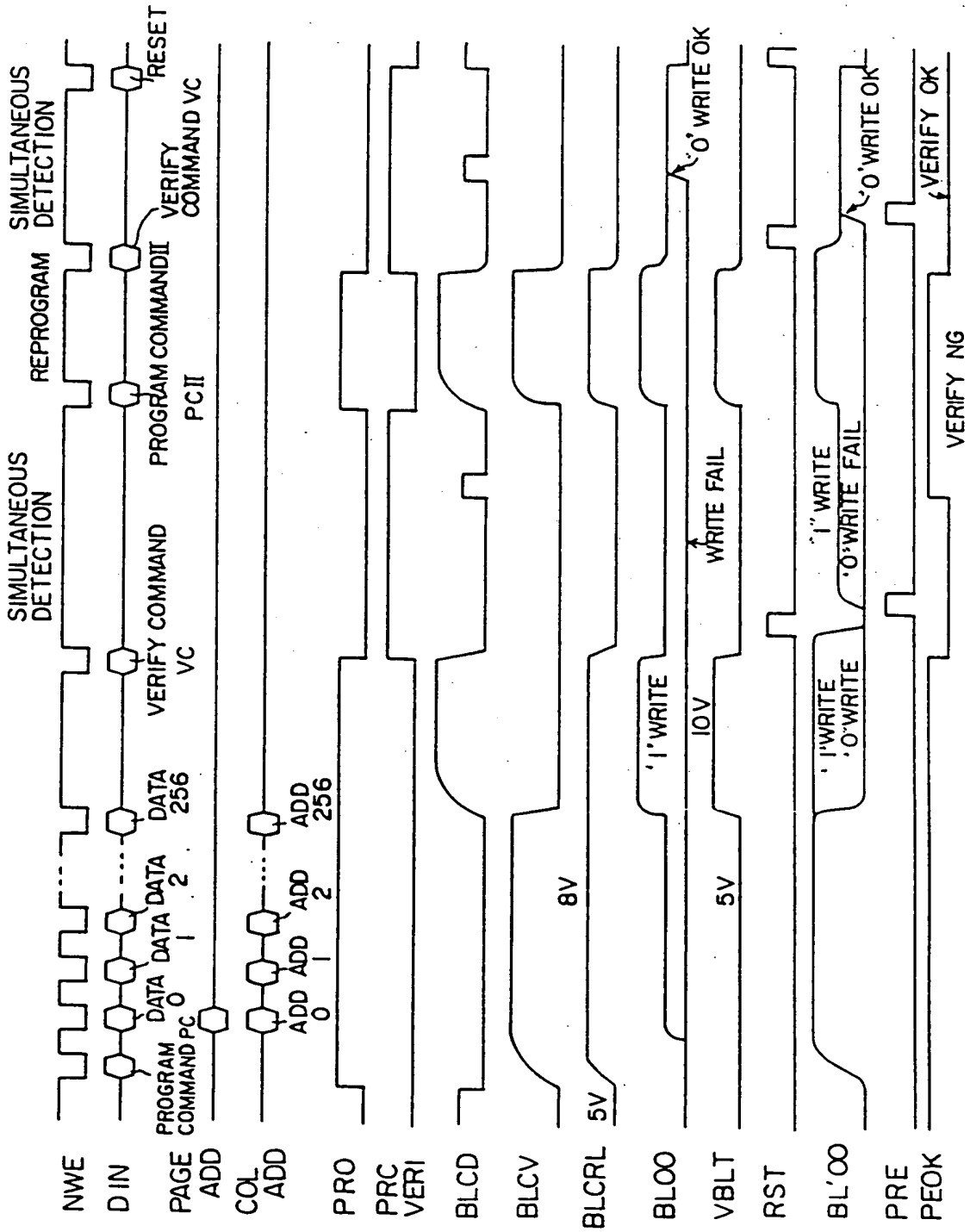

NWE
DIN
PAGE ADD
COL ADD
PRO
PRC VERI
BLCD
BLCV
BLCRL
BLOO
VBLT
RST
BL'OO
PRE
PEOK
PROGRAM COMMAND PC
DATA 0
DATA 1
DATA 2
DATA 256
ADD 0
ADD 1
ADD 2
ADD 256
SIMULTANEOUS DETECTION
VERIFY COMMAND VC
PROGRAM COMMAND PC II
REPROGRAM
SIMULTANEOUS DETECTION
VERIFY COMMAND VC
RESET
8V
5V
5V
'1' WRITE
'0' WRITE
10V
WRITE FAIL
'1' WRITE
'0' WRITE FAIL
'0' WRITE OK
'0' WRITE OK
VERIFY NG
VERIFY OK

FIG. 59

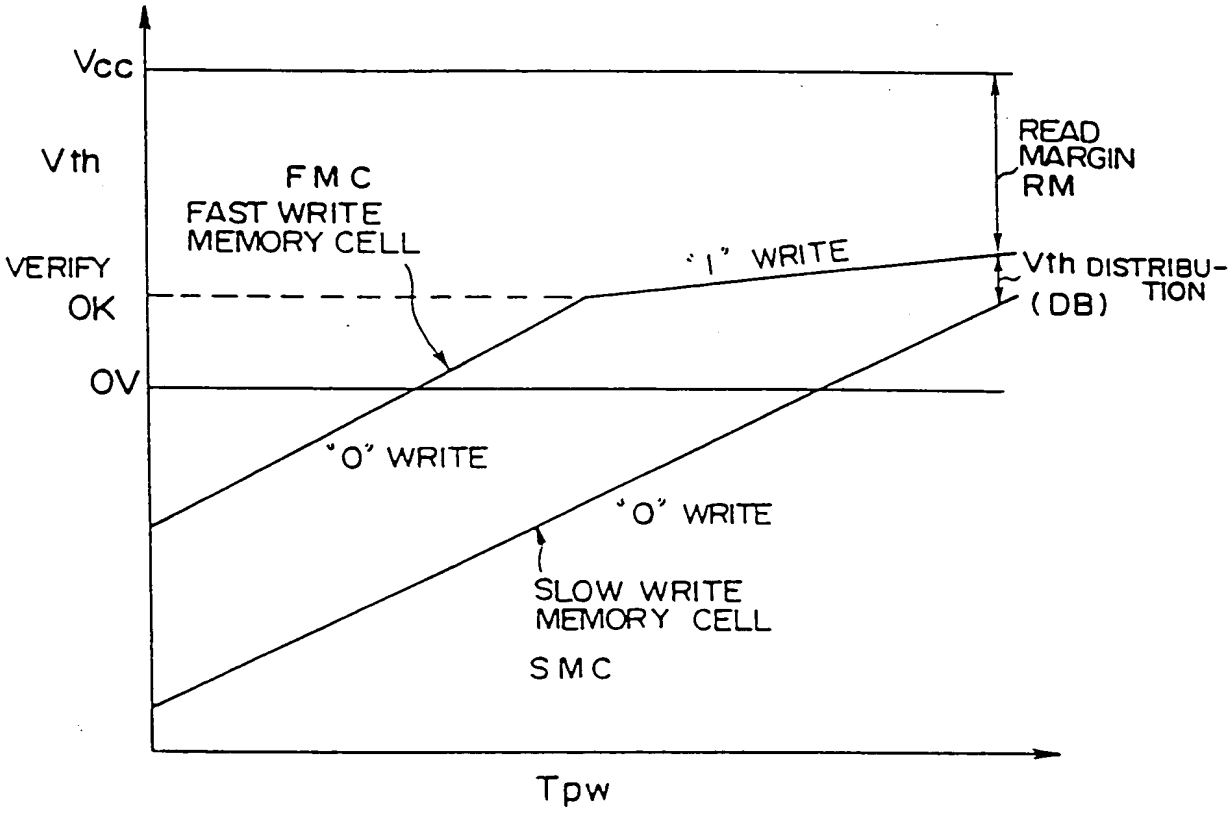

Vcc
Vth
FMC
FAST WRITE
MEMORY CELL
VERIFY
OK
OV
"1" WRITE
"0" WRITE
"0" WRITE
SLOW WRITE
MEMORY CELL
SMC
READ
MARGIN
RM
Vth DISTRIBU-
TION
(DB)
Tpw

FIG. 60

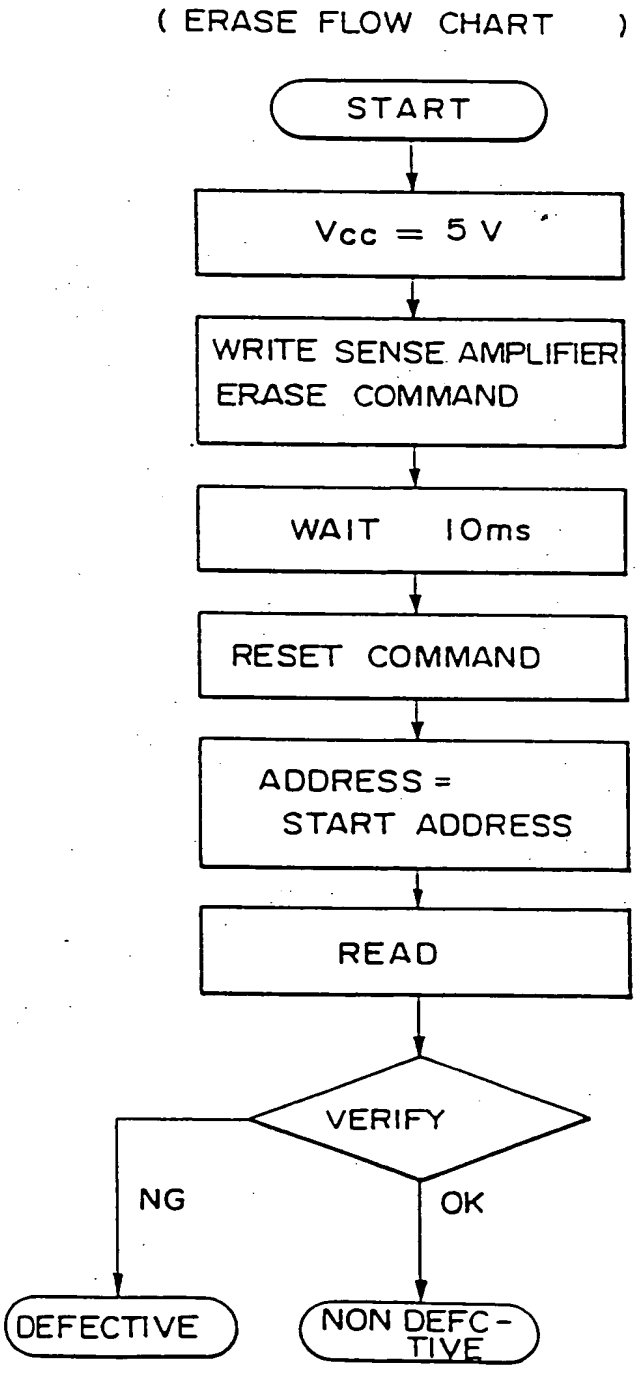

(ERASE FLOW CHART)
START
Vcc = 5 V
WRITE SENSE AMPLIFIER ERASE COMMAND
WAIT 10ms
RESET COMMAND
ADDRESS = START ADDRESS
READ
VERIFY
NG
OK
DEFECTIVE
NON DEFC-TIVE

FIG. 61

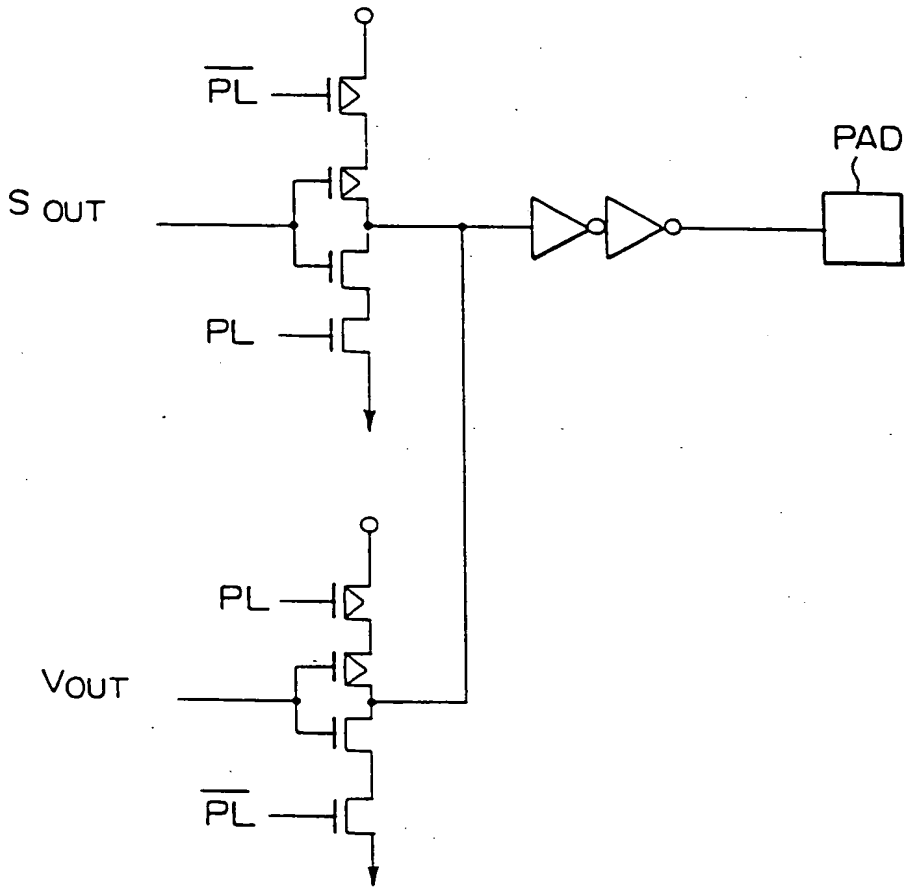


FIG. 62

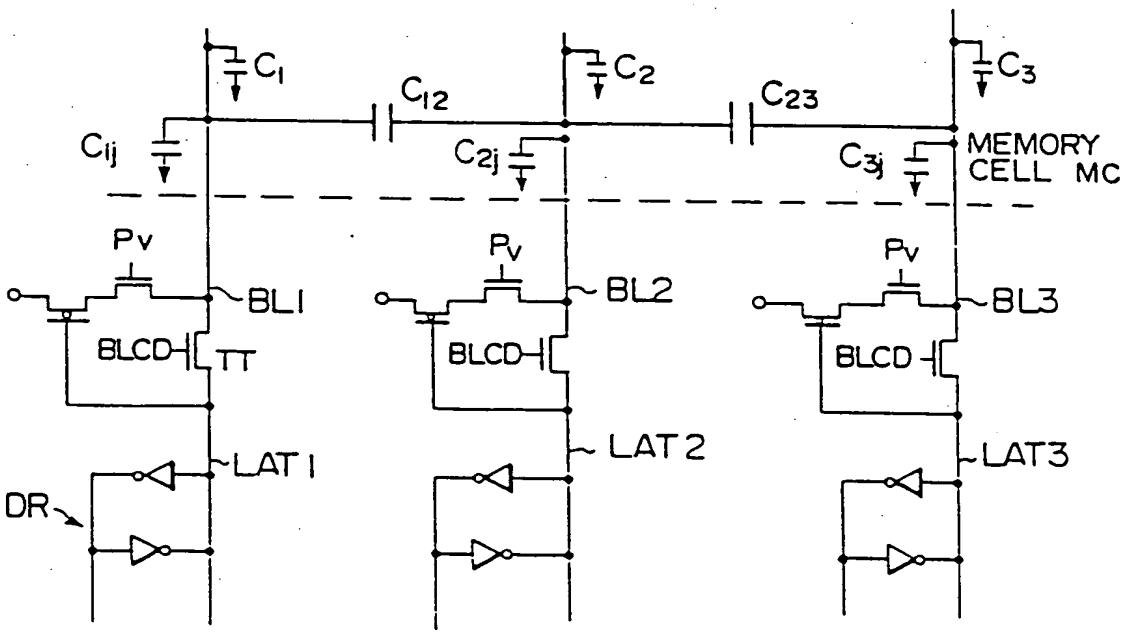

C1
C12
C2
C23
C3
Cij
C2j
C3j
MEMORY
CELL MC
Pv
Pv
Pv
BL1
BL2
BL3
BLCD
TT
BLCD
BLCD
LAT1
LAT2
LAT3
DR

FIG. 63

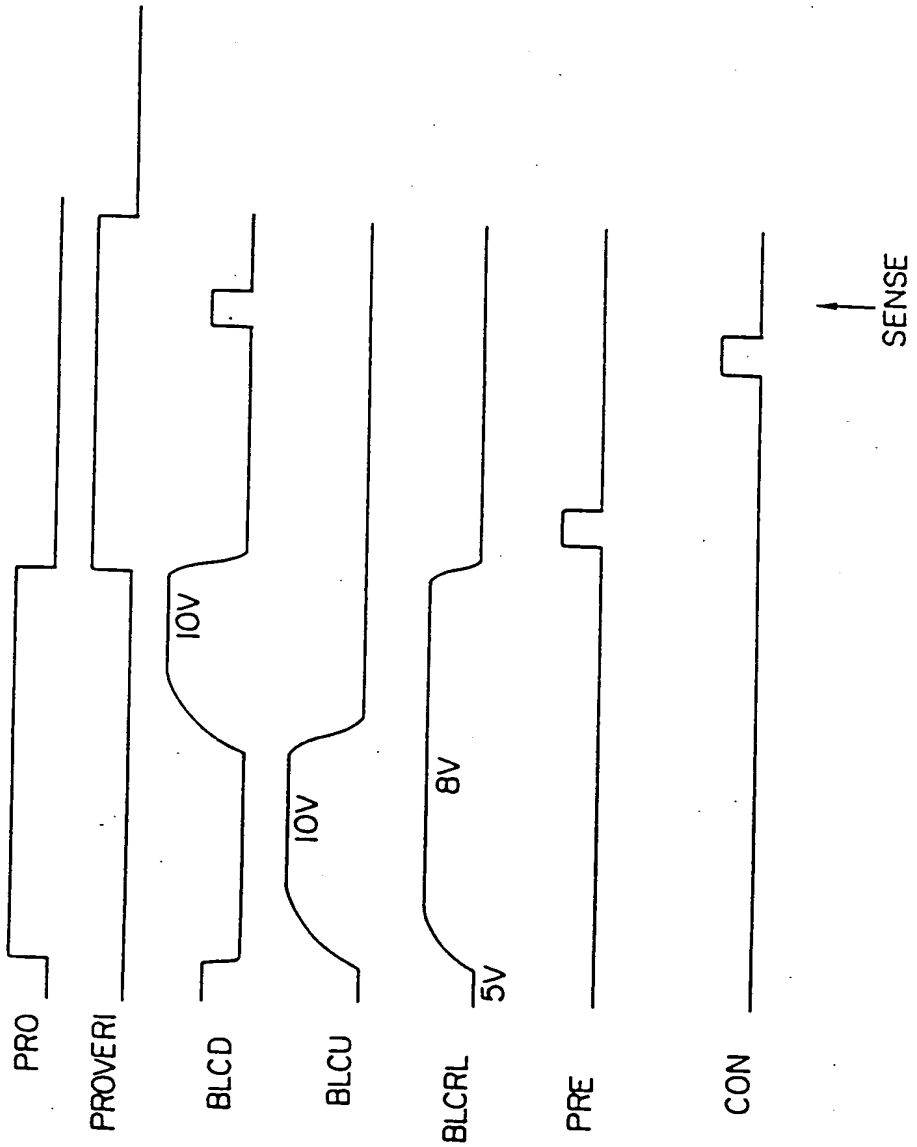


FIG.64

FIG. 65(a)

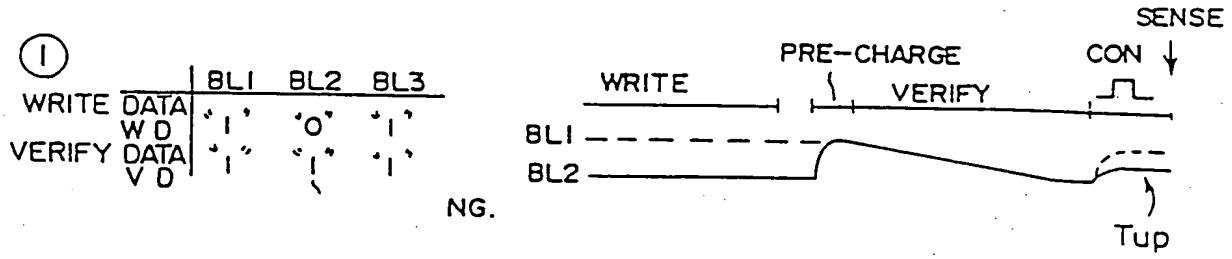


FIG. 65(b)

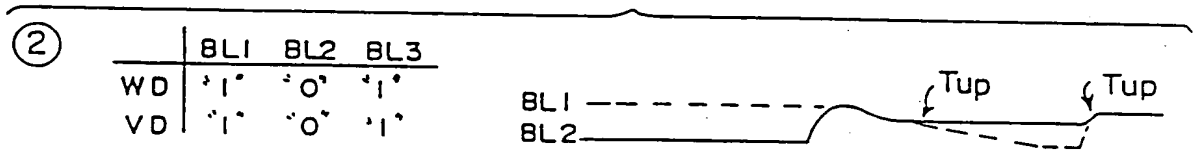


FIG. 65(c)

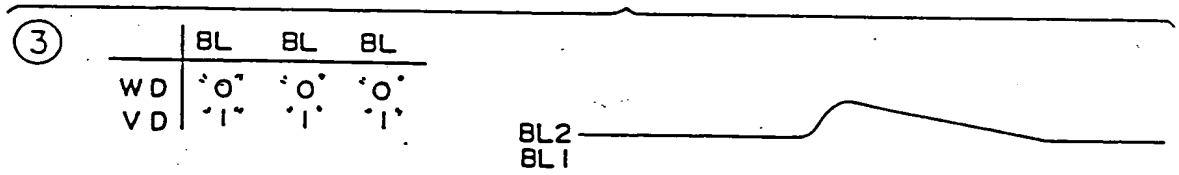


FIG. 65(d)

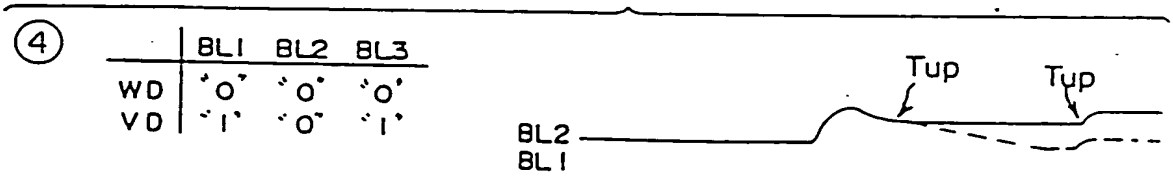


FIG. 65(e)

⑤

	BL1	BL2	BL3
WD	"0"	"0"	"0"
VD	"0"	"1"	"0"

FIG. 65(f)

⑥

	BL1	BL2	BL3
WD	"0"	"0"	"0"
VD	"0"	"0"	"0"

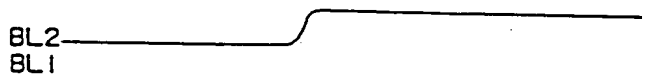


FIG. 65(g)

⑦

	BL1	BL2	BL3
WD	"0"	"1"	"0"
VD	"1"	"1"	"1"

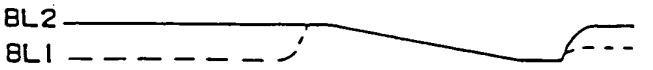


FIG. 65(h)

⑧

	BL1	BL2	BL3
WD	"0"	"1"	"0"
VD	"0"	"1"	"0"

FIG. 66(a)

	BL1	BL2	BL3
WD	"1"	"0"	"1"
VD	"1"	"1"	"1"

FIG. 66(b)

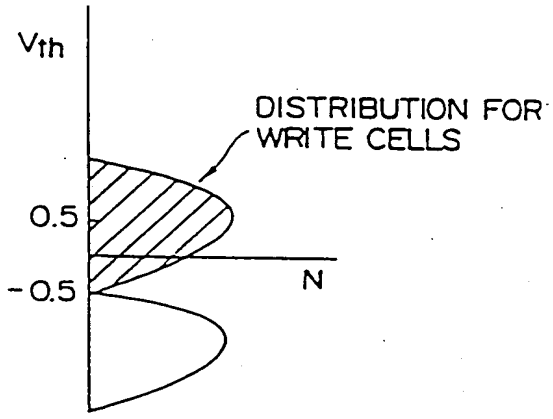
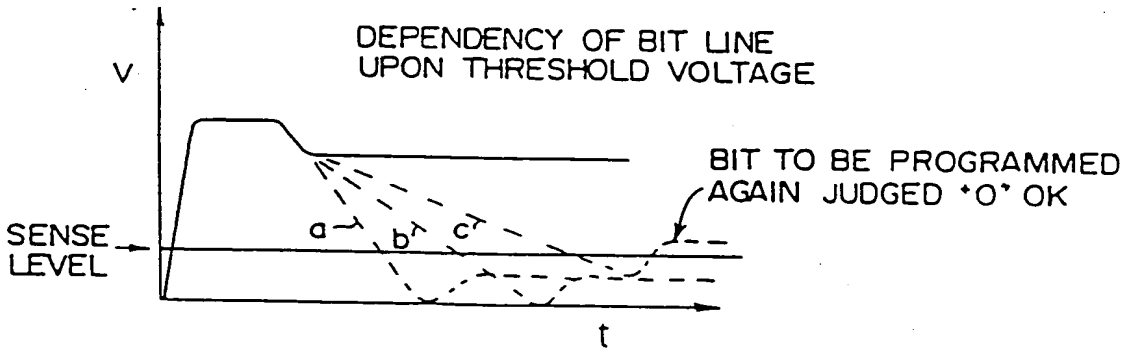


FIG. 66(c)



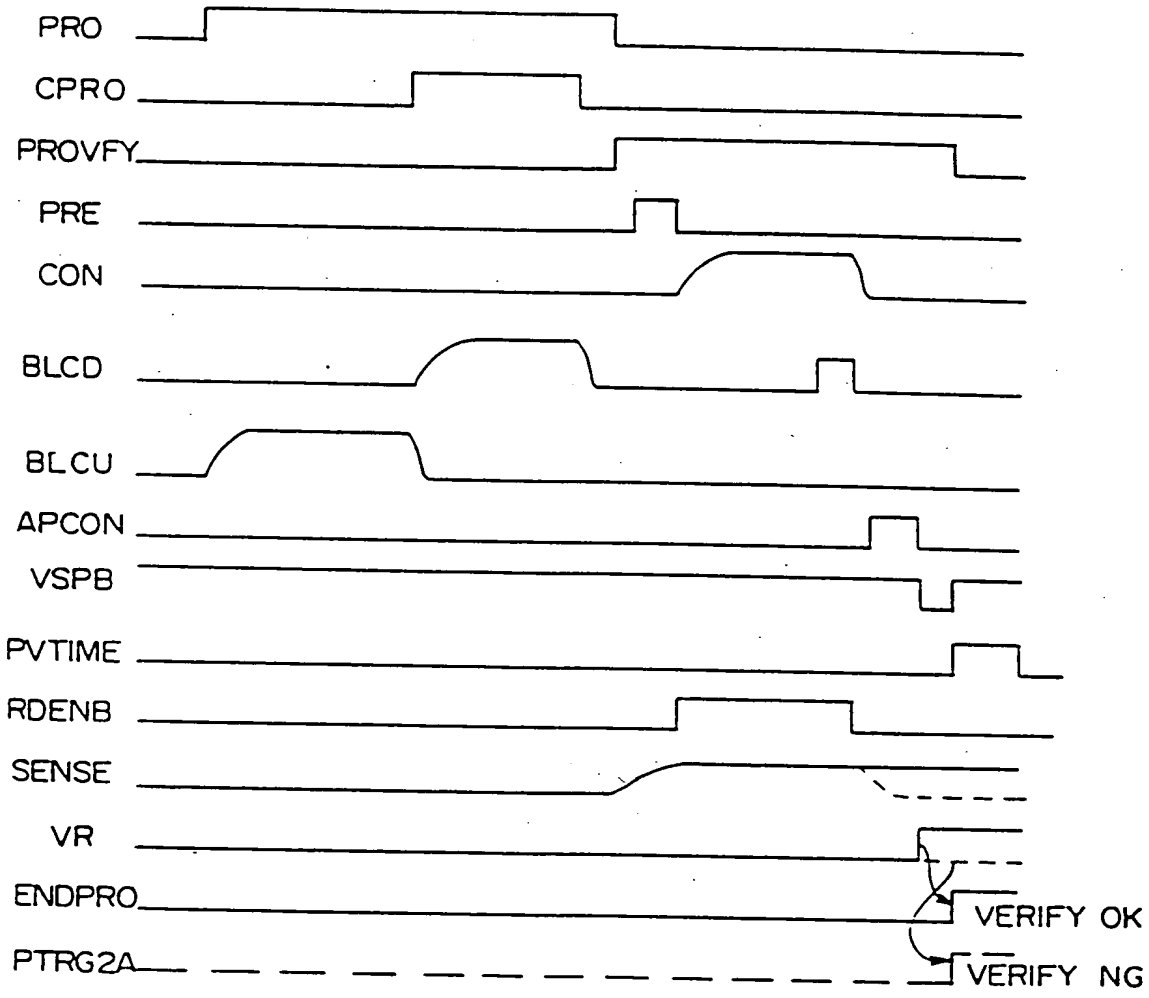

PRO
CPRO
PROVFY
PRE
CON
BLCD
BLCU
APCON
VSPB
PVTIME
RDENB
SENSE
VR
ENDPRO
PTRG2A
VERIFY OK
VERIFY NG

FIG. 67

FIG. 68(a)

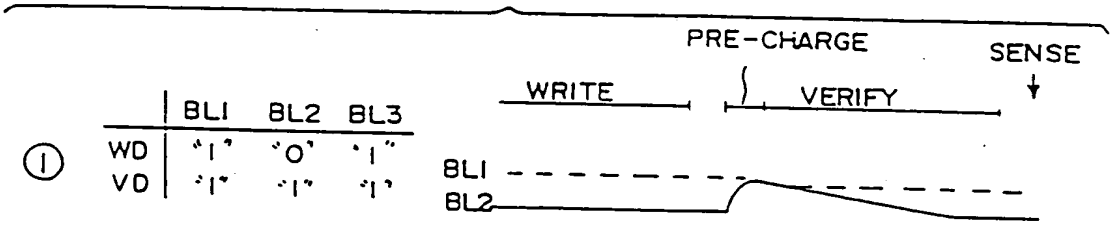


FIG. 68(b)

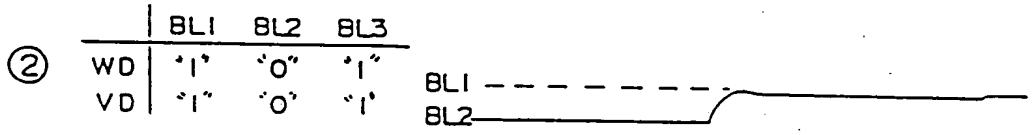


FIG. 68(c)

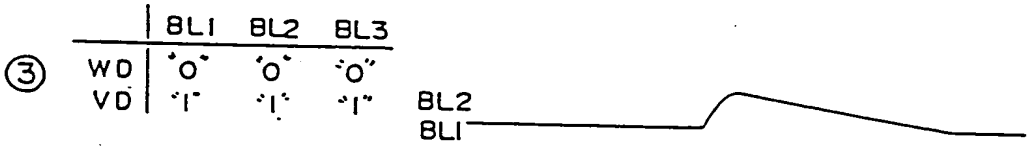


FIG. 68(d)

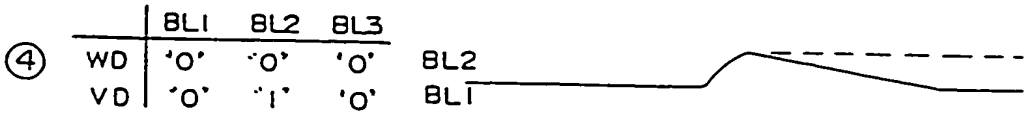


FIG. 68(e)

⑤		BL1	BL2	BL3
	WD	'0'	'0'	'0'
	VD	'1'	'0'	'1'

FIG. 68(f)

⑥		BL1	BL2	BL3
	WD	'0'	'0'	'0'
	VD	'0'	'0'	'0'

FIG. 68(g)

⑦		BL1	BL2	BL3
	WD	'0'	'1'	'0'
	VD	'1'	'1'	'1'

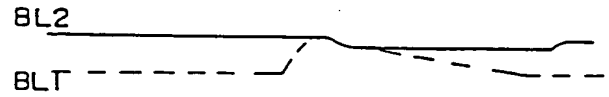


FIG. 68(h)

⑧		BL1	BL2	BL3
	WD	'0'	'1'	'0'
	VD	'0'	'1'	'0'

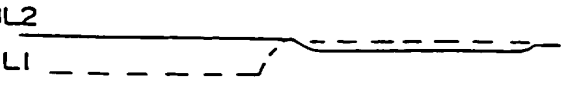


FIG. 69(a)

	BL1	BL2	BL3
WD	"1"	"0"	"1"
VD	"1"	"1"	"1"

FIG. 69(b)

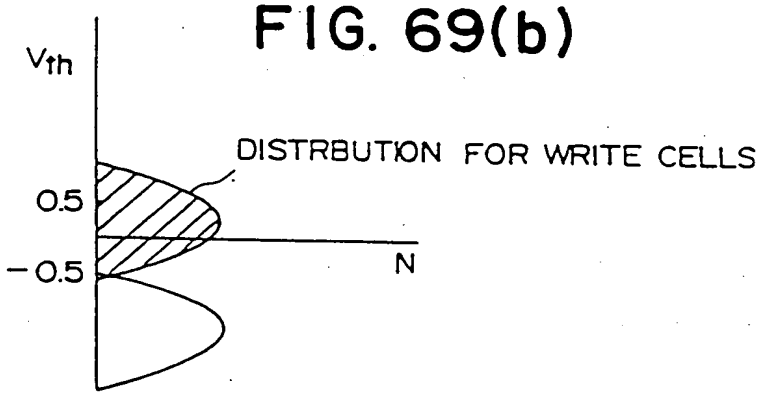


FIG. 69(c)

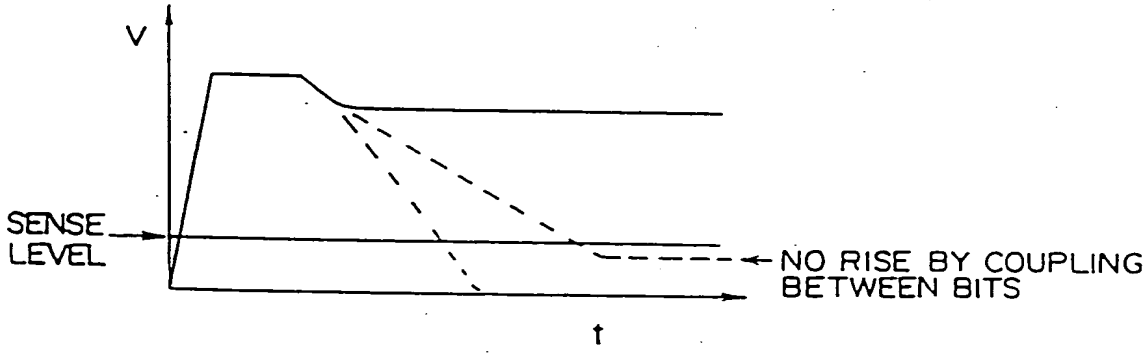


FIG. 70(a)

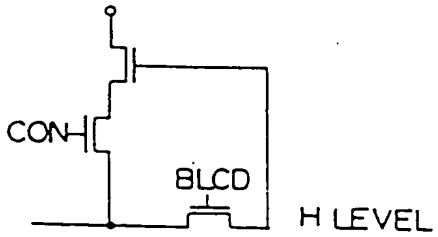


FIG. 70(b)

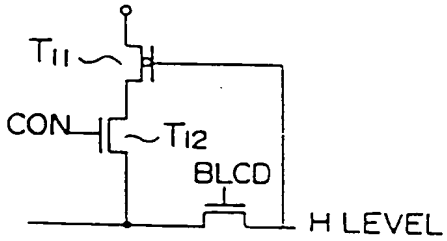
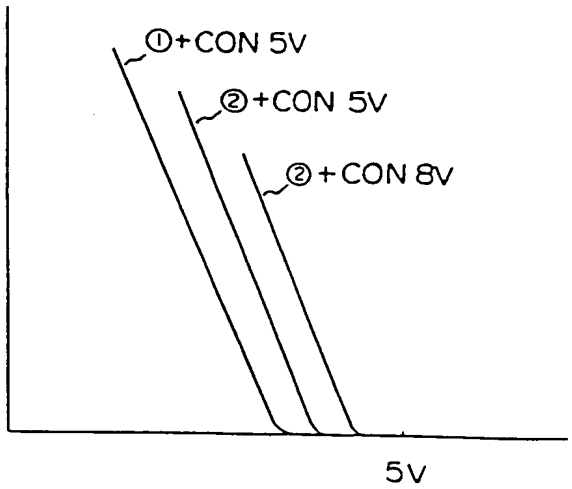


FIG. 70(c)



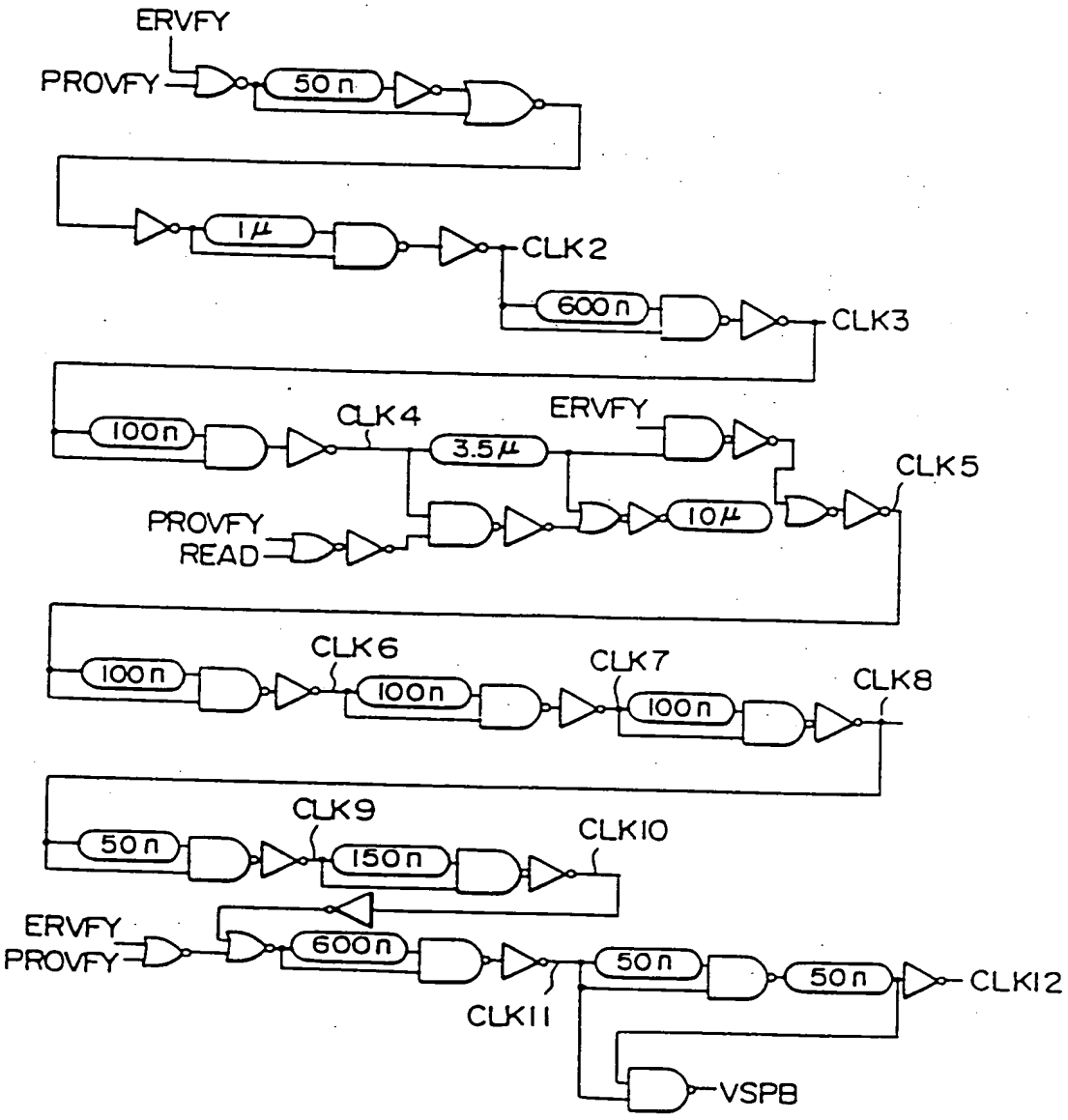

ERVFY
PROVFY
50n
1μ
CLK2
600n
CLK3
100n
CLK4
3.5μ
ERVFY
CLK5
10μ
PROVFY
READ
CLK6
100n
CLK7
100n
CLK8
100n
CLK9
50n
150n
CLK10
ERVFY
PROVFY
600n
CLK11
50n
50n
CLK12
VSPB

FIG. 71

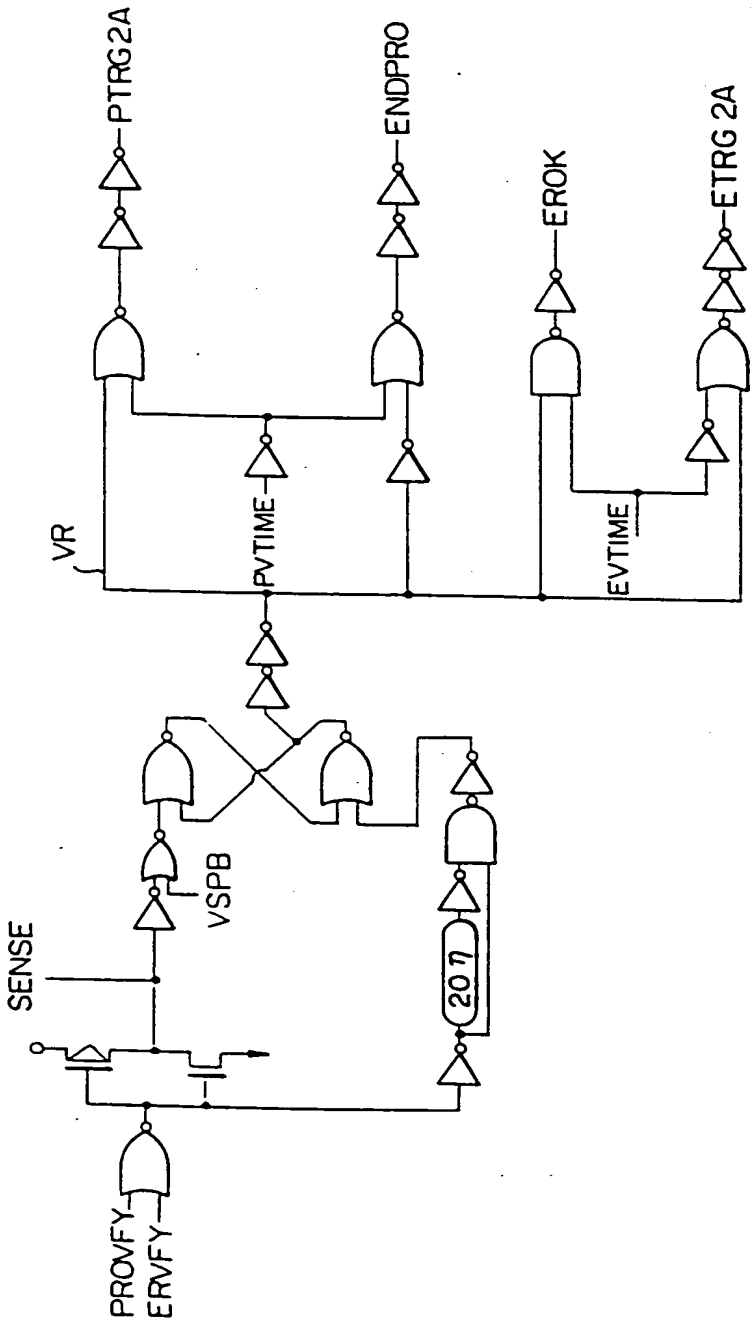

PTRG2A
ENDPRO
EROK
ETRG2A
VR
PVTIME
EVTIME
VSPB
SENSE
20n
PROVFY
ERVFY

FIG. 72

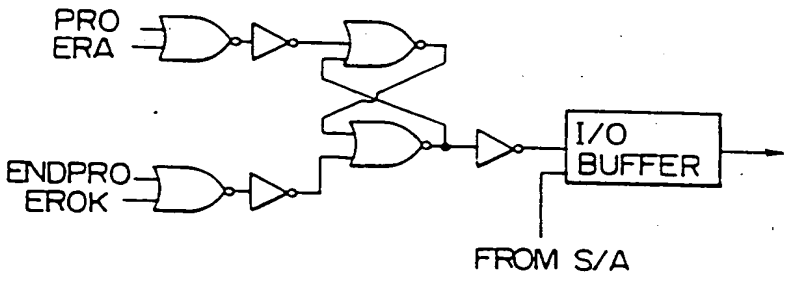


FIG. 73

FIG. 74(a)

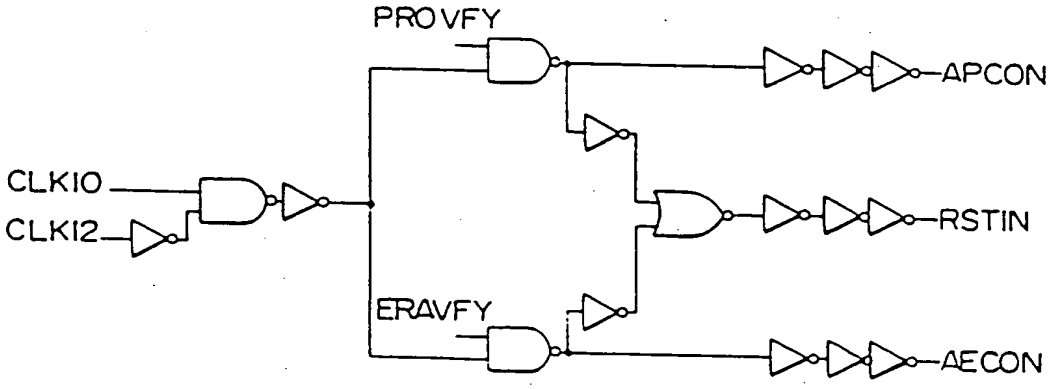


FIG. 74(b)

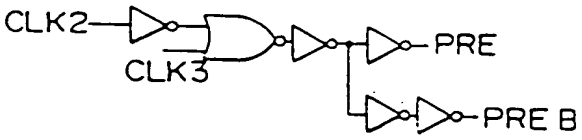
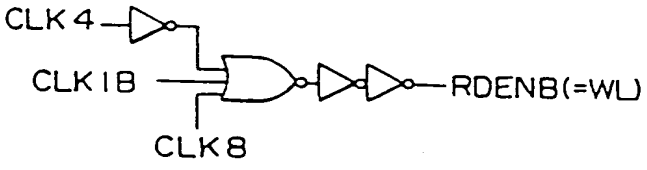


FIG. 74(c)



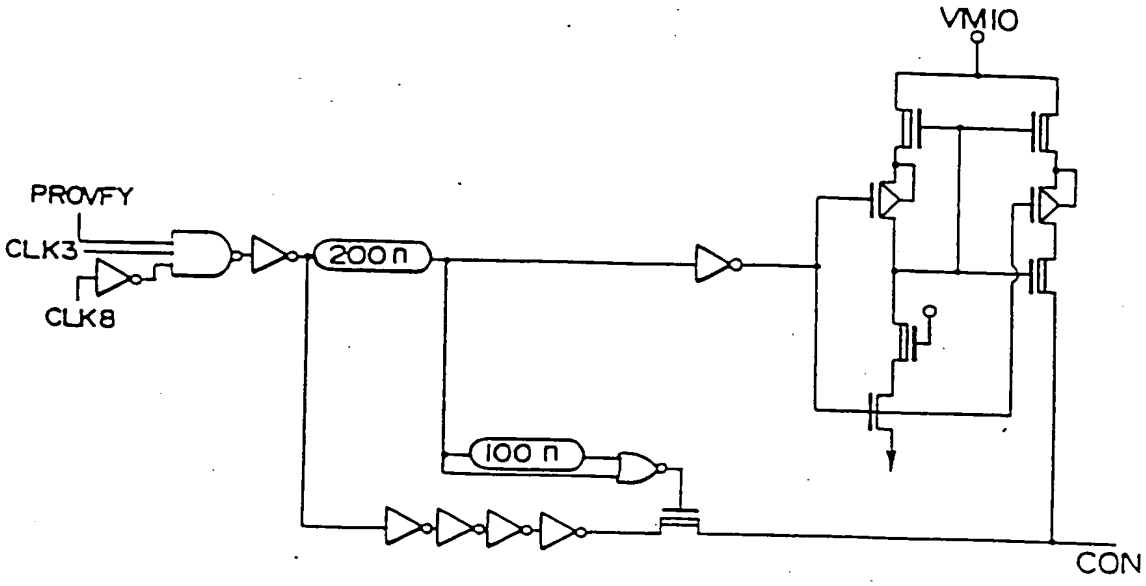


FIG. 75

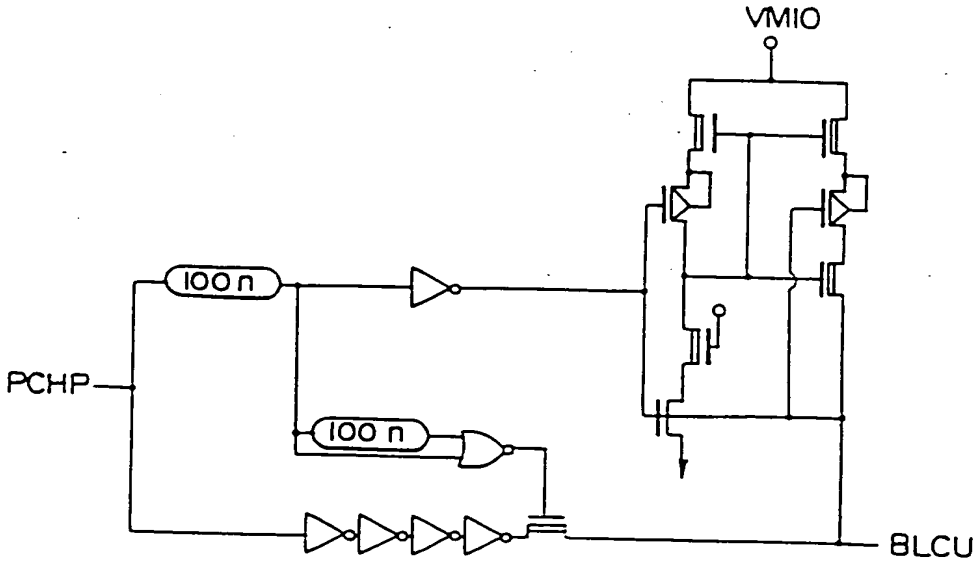


FIG. 76

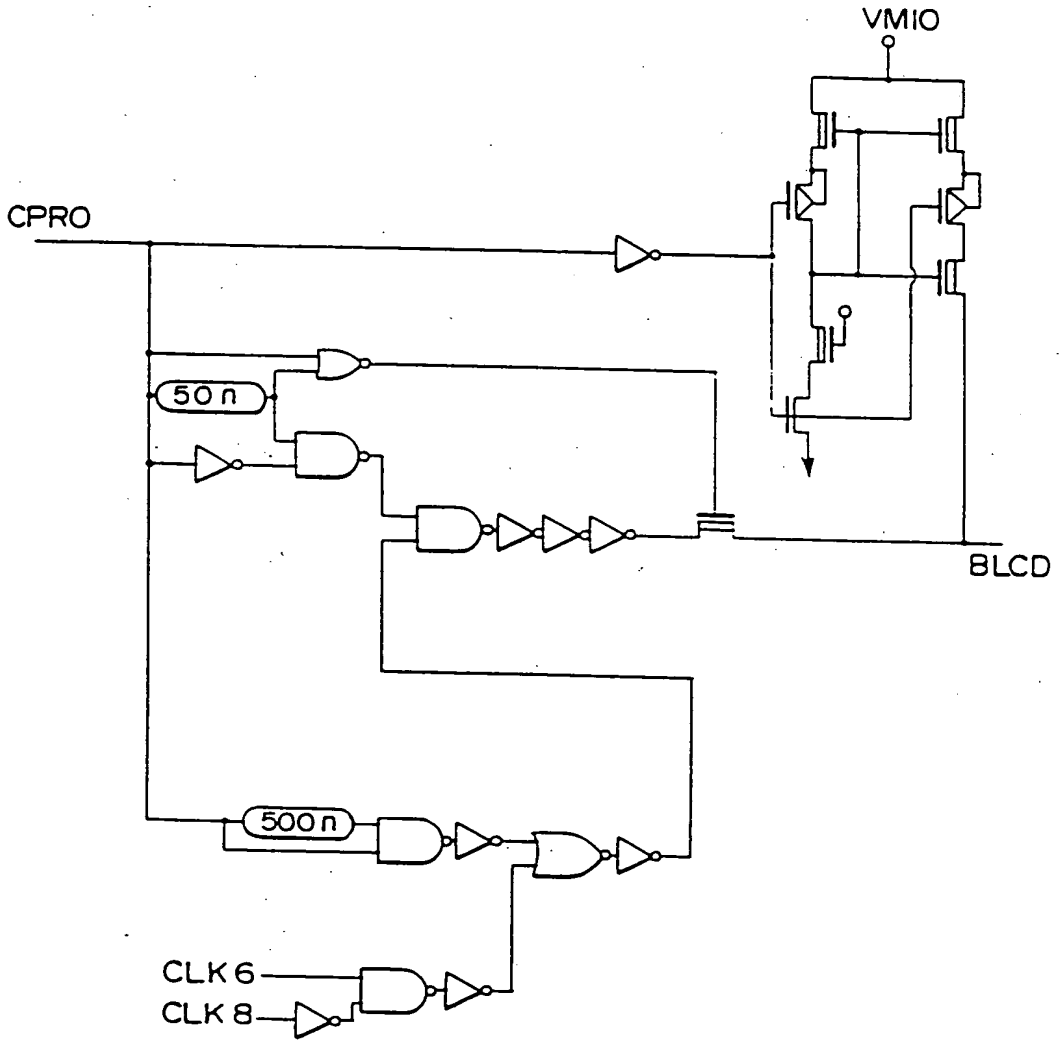


FIG. 77

FIG. 78(a)

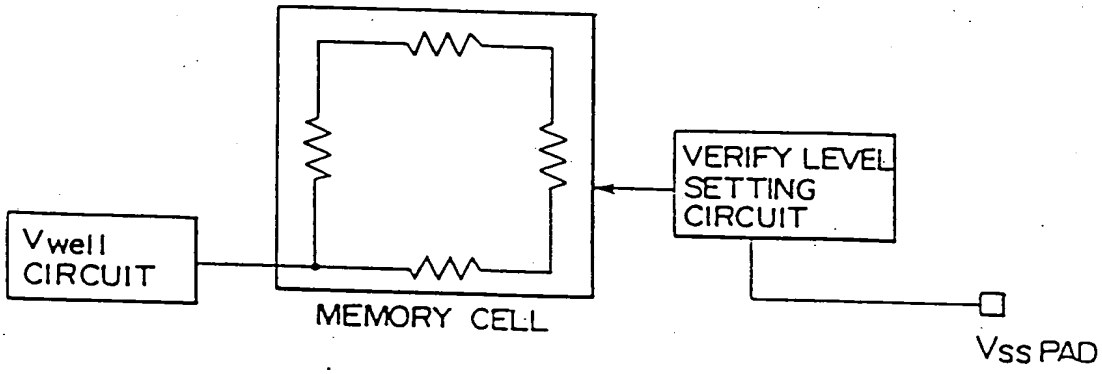
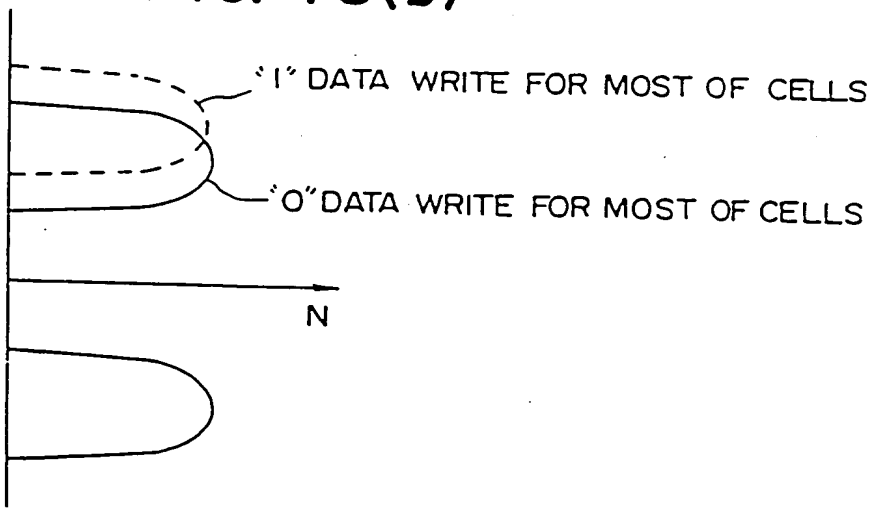


FIG. 78(b)



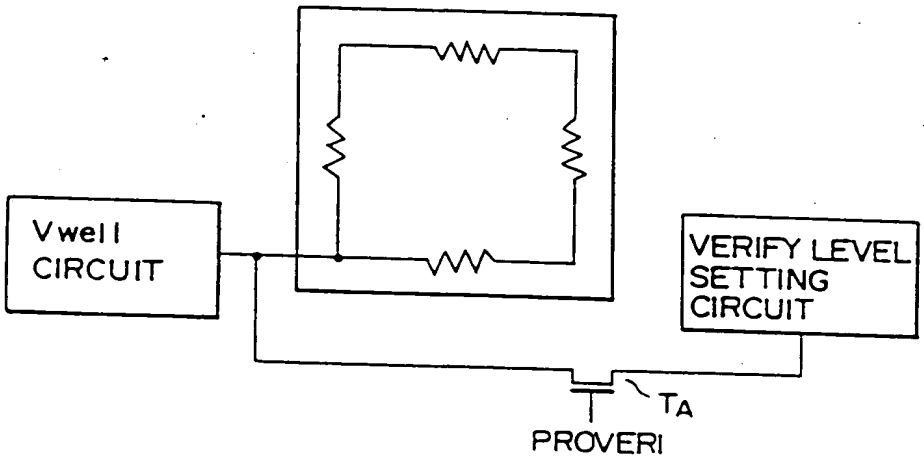


FIG. 79

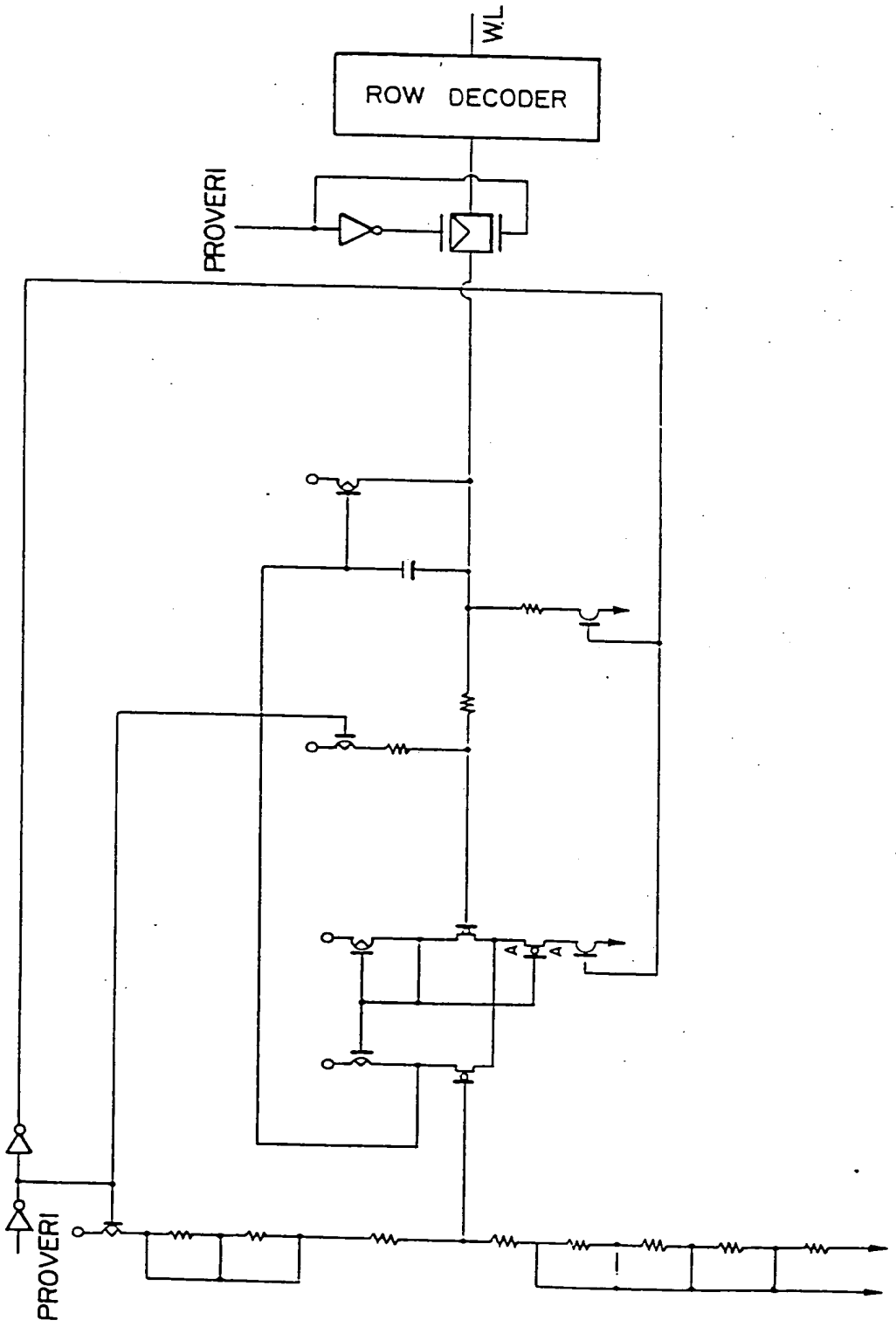


FIG. 80

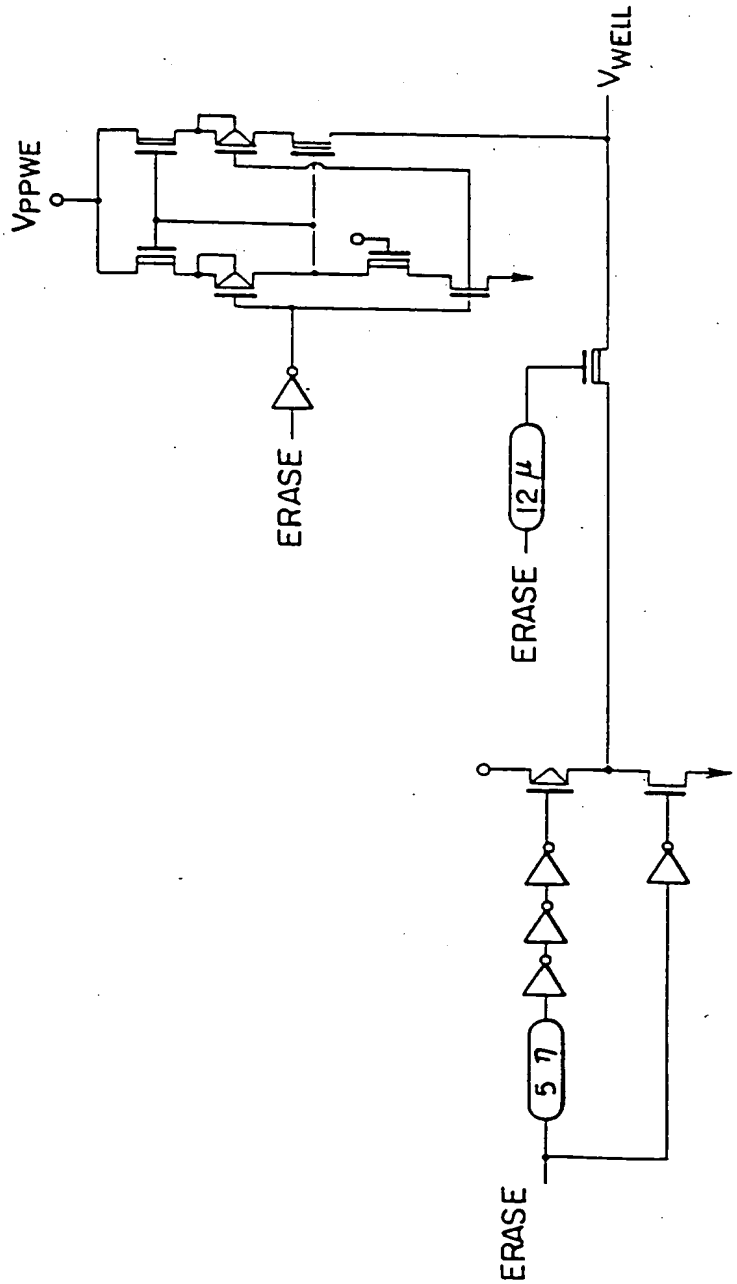


FIG. 81

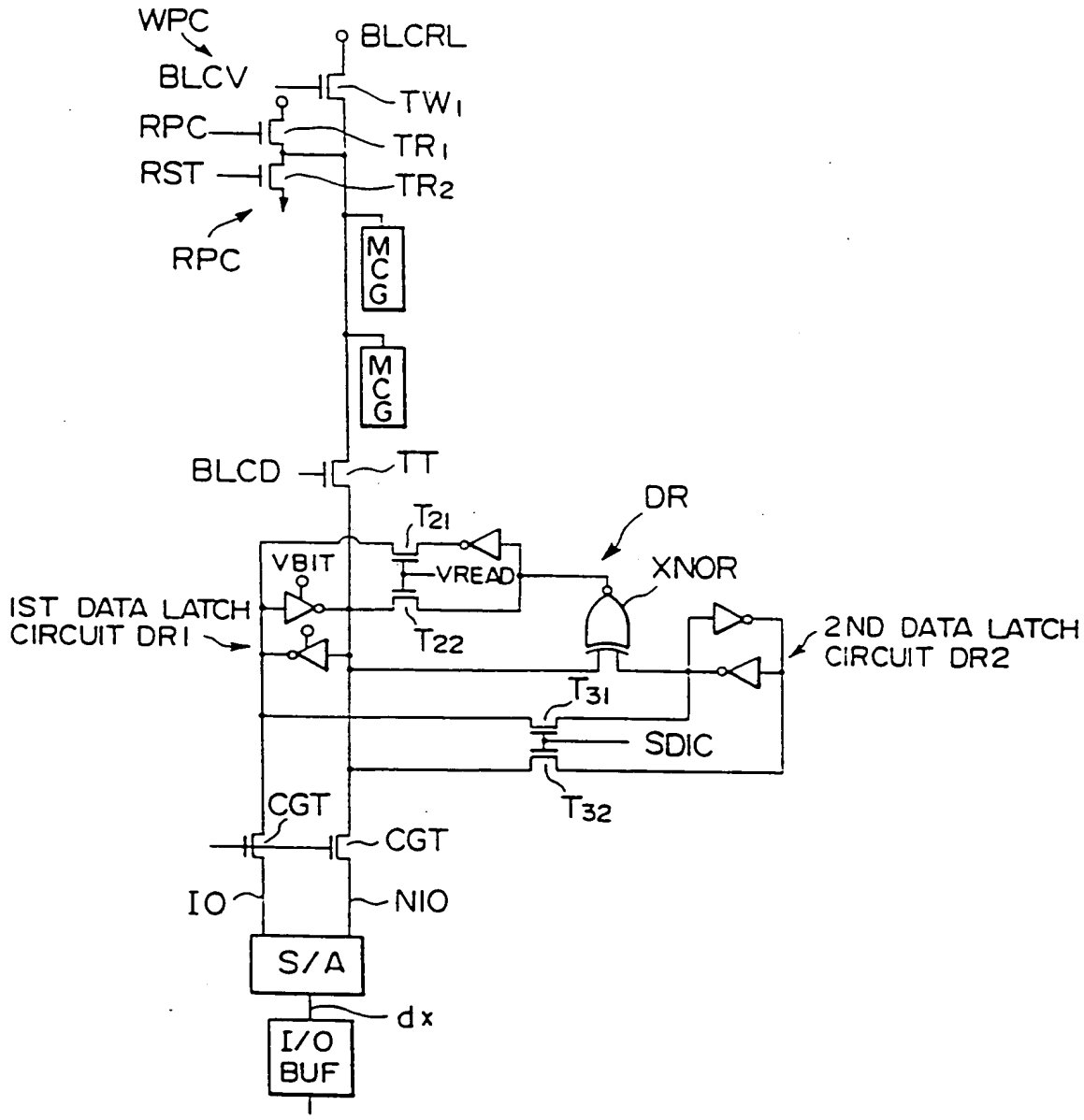


FIG. 82

WRITE DATA	0	0	1	1
VERIFY DATA	0	1	0	1
OUTPUT DATA AFTER COMPARISON	0	1	1	0

FIG. 83

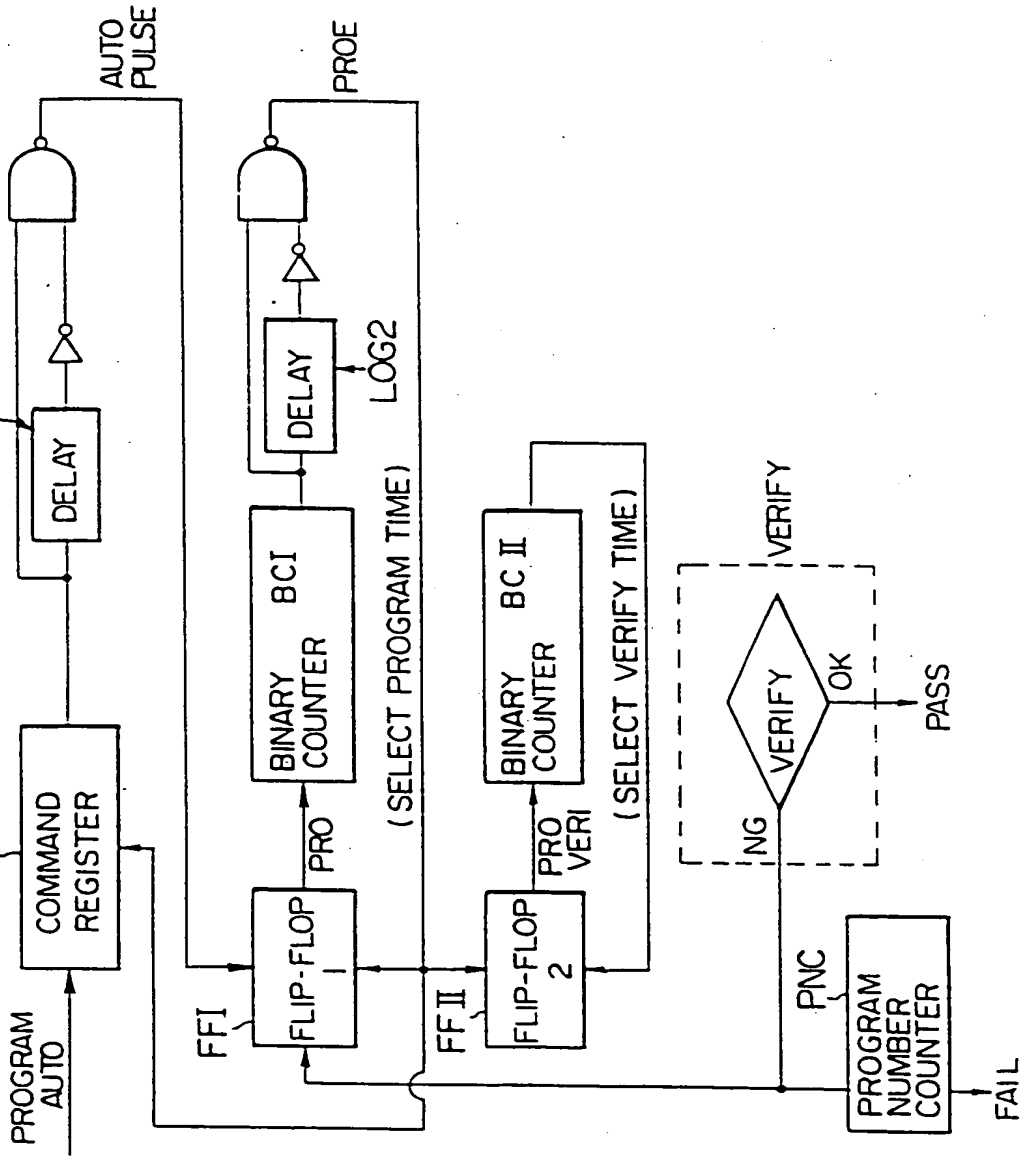

AUTO PULSE
PROE
LOGI
LOG2
DELAY
DELAY
CR
COMMAND REGISTER
BINARY COUNTER BCI
BINARY COUNTER BC II
PRO
PRO VERI
(SELECT PROGRAM TIME)
(SELECT VERIFY TIME)
FFI
FF II
FLIP-FLOP 1
FLIP-FLOP 2
VERIFY
VERIFY
OK
NG
PASS
PNC
PROGRAM NUMBER COUNTER
FAIL
PROGRAM AUTO

FIG. 84

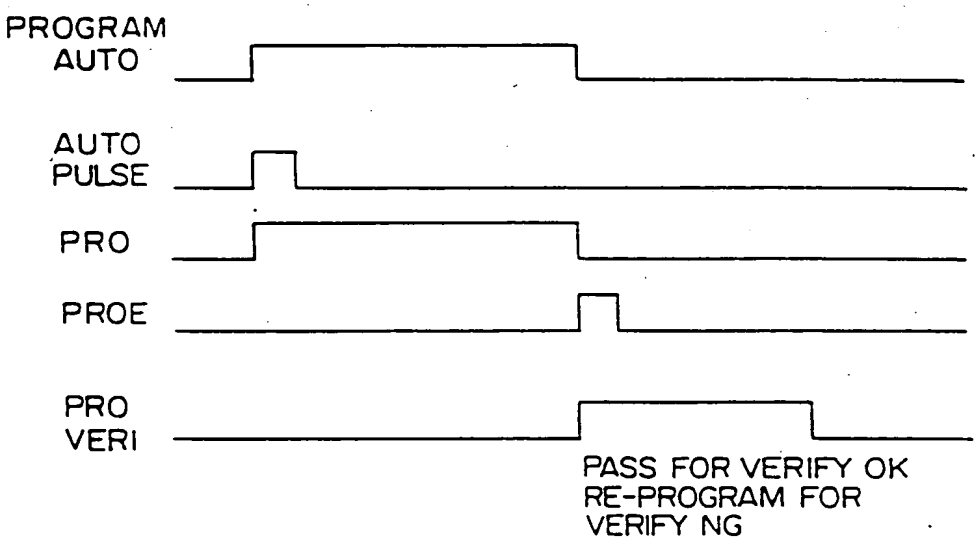

PROGRAM
AUTO
AUTO
PULSE
PRO
PROE
PRO
VERI
PASS FOR VERIFY OK
RE-PROGRAM FOR
VERIFY NG

FIG. 85

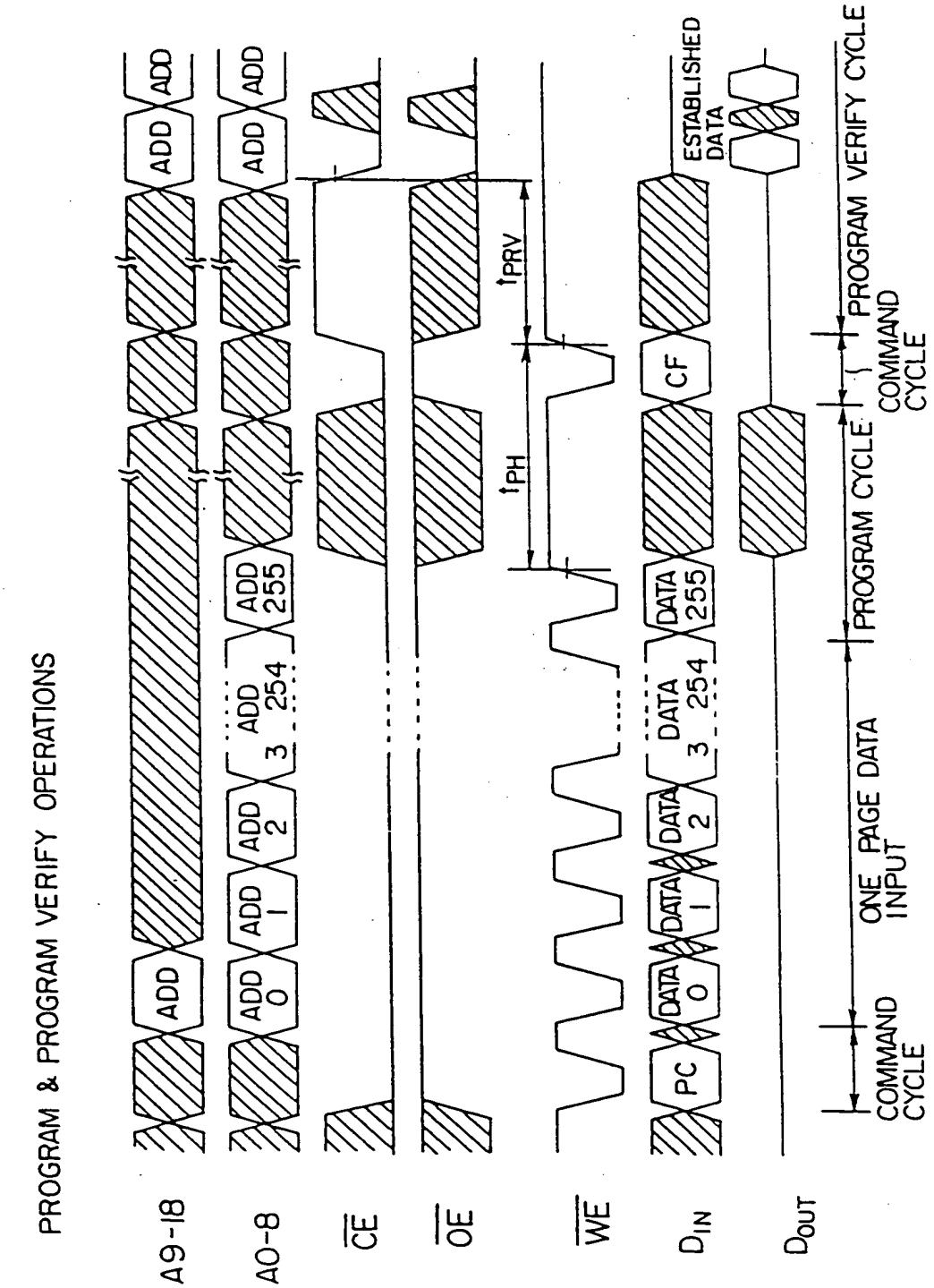

PROGRAM & PROGRAM VERIFY OPERATIONS
A9-18
A0-8
CE
OE
WE
DIN
DOUT
ADD
ADD 0
ADD 1
ADD 2
ADD 3
ADD 254
ADD 255
PC
DATA 0
DATA 1
DATA 2
DATA 3
DATA 254
DATA 255
CF
ESTABLISHED DATA
tPRV
tPH
COMMAND CYCLE
ONE PAGE DATA INPUT
PROGRAM CYCLE
PROGRAM VERIFY CYCLE
COMMAND CYCLE

FIG. 86

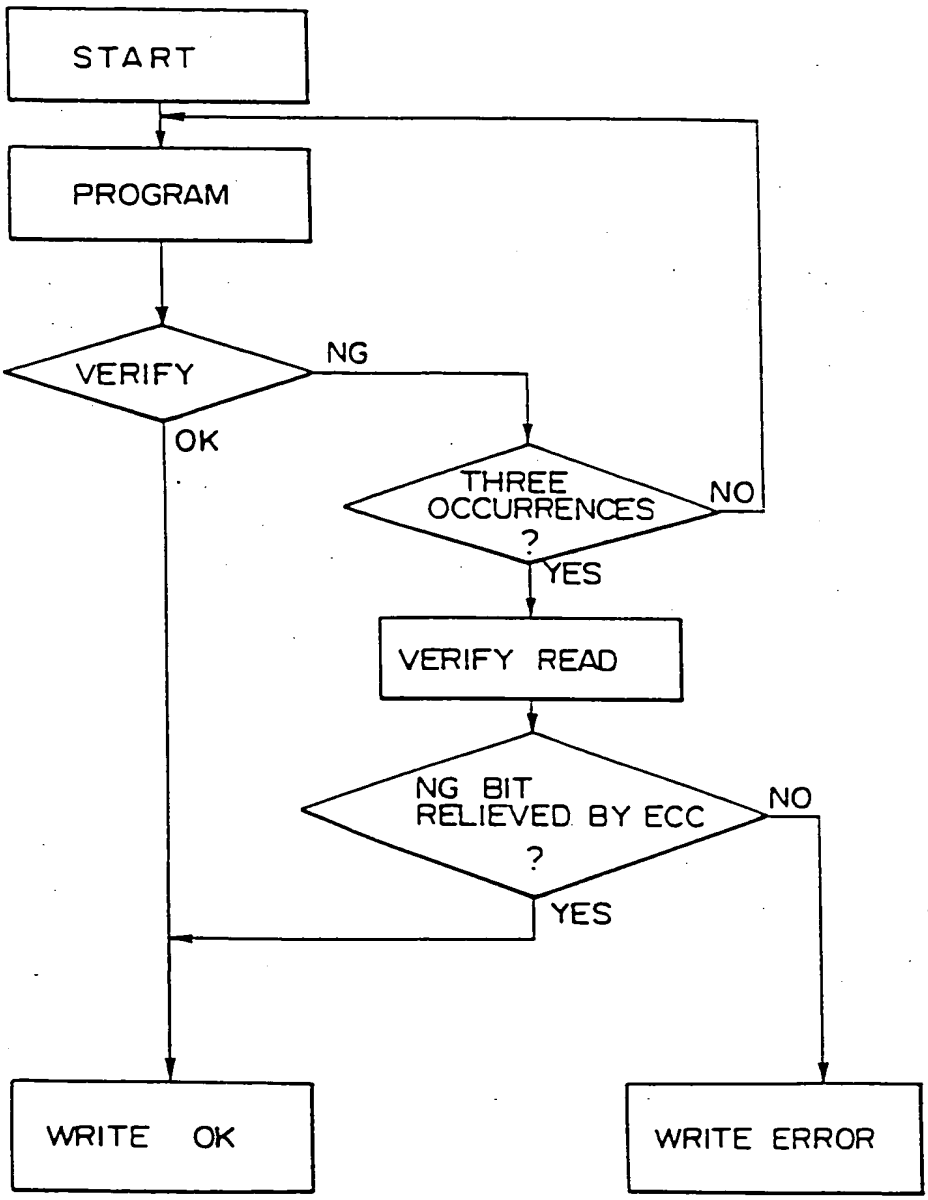

START
PROGRAM
VERIFY
NG
OK
THREE OCCURRENCES ?
NO
YES
VERIFY READ
NG BIT RELIEVED BY ECC ?
NO
YES
WRITE OK
WRITE ERROR

FIG. 87

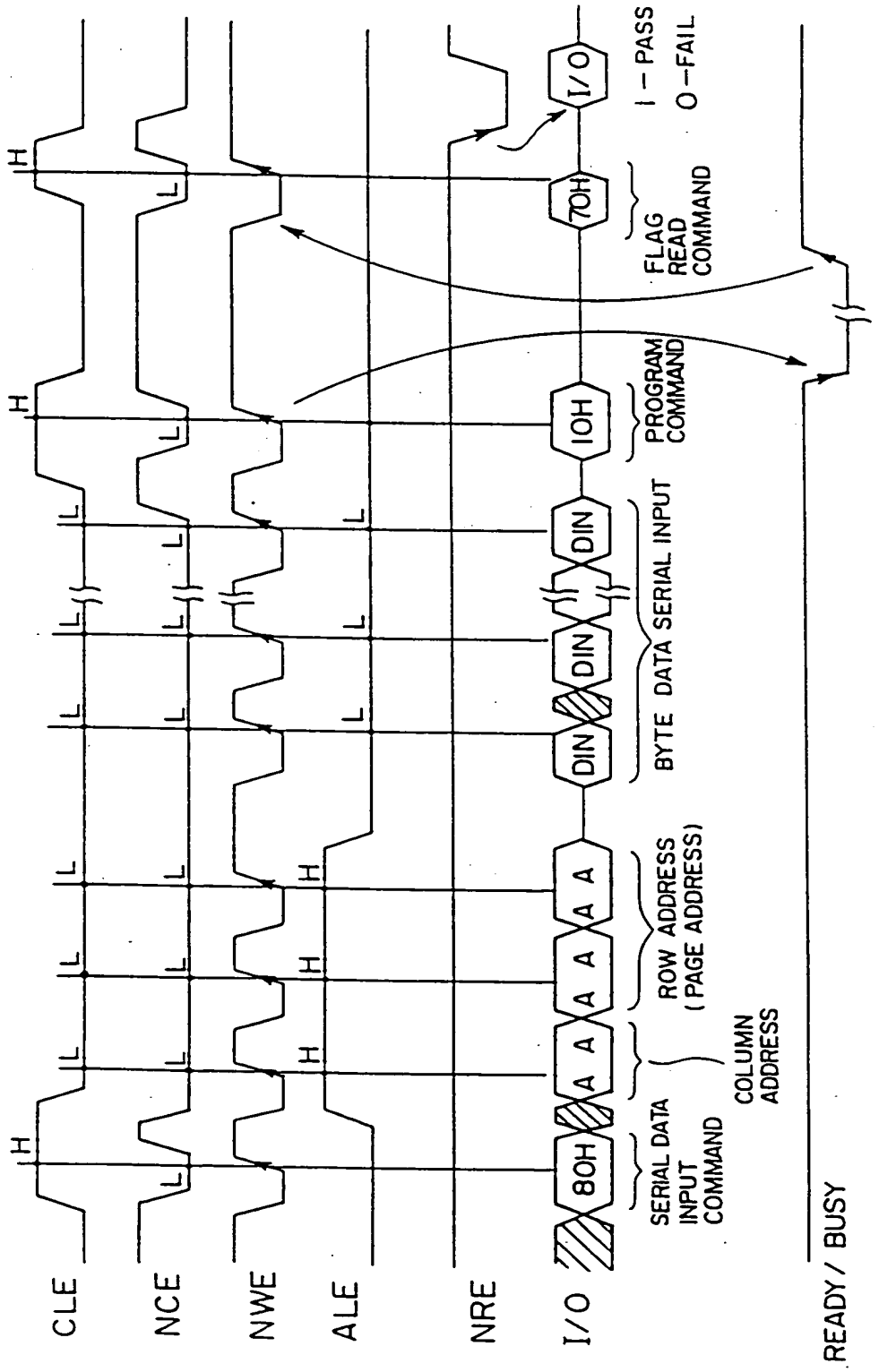

CLE
NCE
NWE
ALE
NRE
I/O
READY / BUSY
80H
A A
A A
A A
DIN
DIN
DIN
10H
70H
I/O
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
FLAG READ COMMAND
I - PASS
O - FAIL

FIG. 88

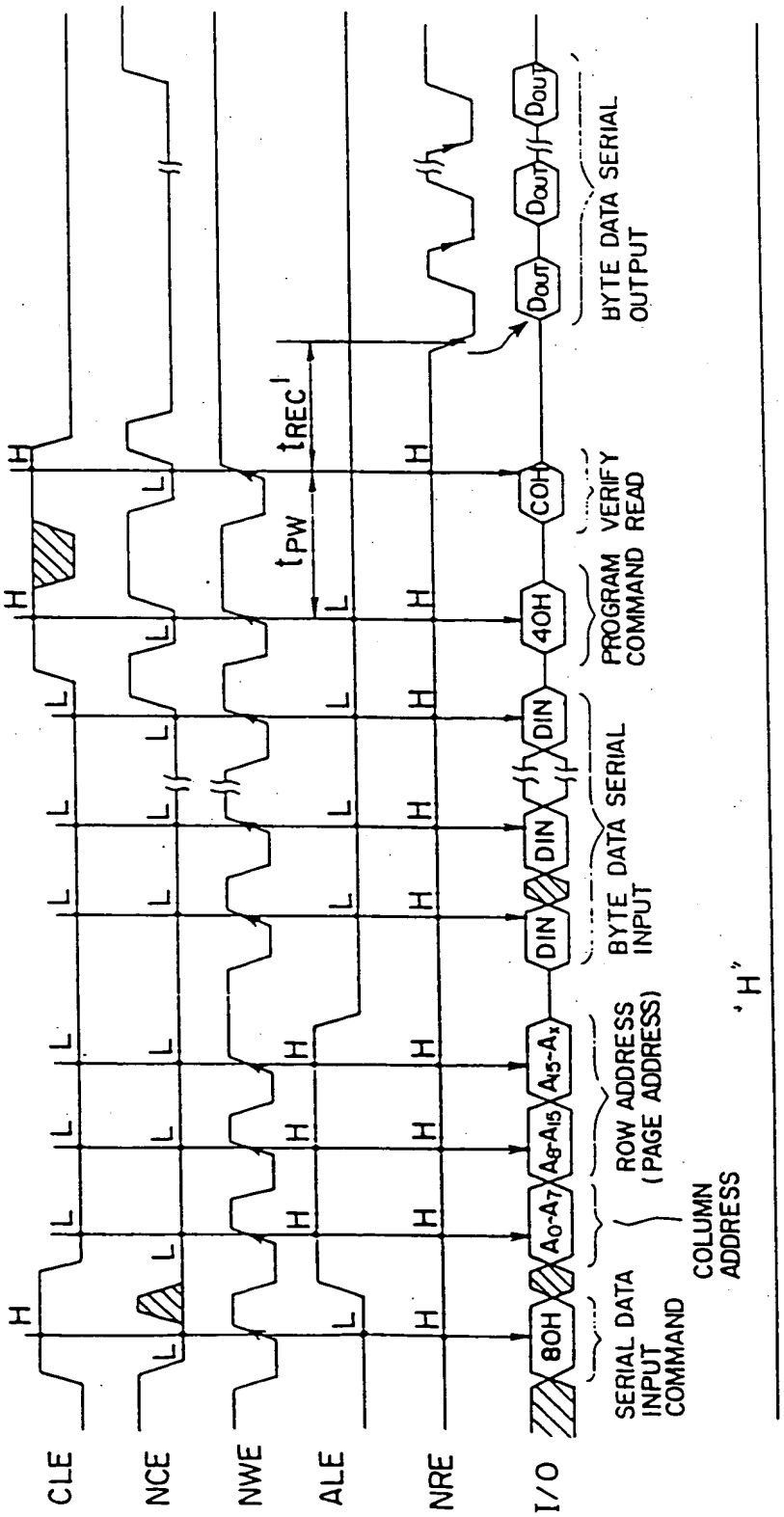

CLE
NCE
NWE
ALE
NRE
I/O
READY / BUSY
H
L
tPW
tREC'
80H
A0-A7
A8-A15
A16-A17
DIN
40H
COH
Dout
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
BYTE DATA SERIAL OUTPUT
'H'

FIG.89

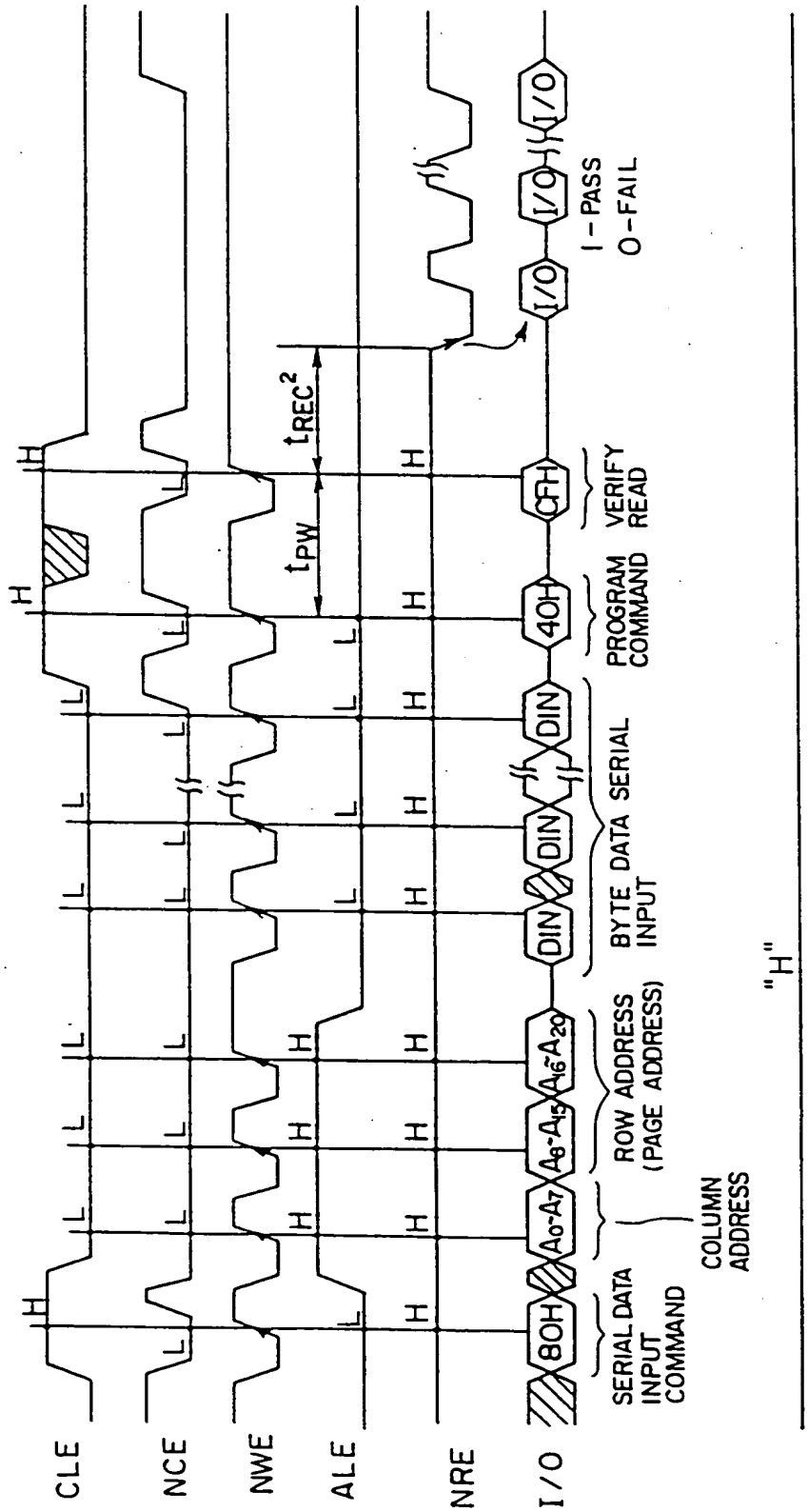

CLE
NCE
NWE
ALE
NRE
I/O
READY / BUSY
"H"
80H
A0-A7
A8-A15
A16-A20
DIN
DIN
DIN
DIN
40H
CFH
I/O
I/O
I/O
tPW
tREC2
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
I - PASS
O - FAIL

FIG. 90

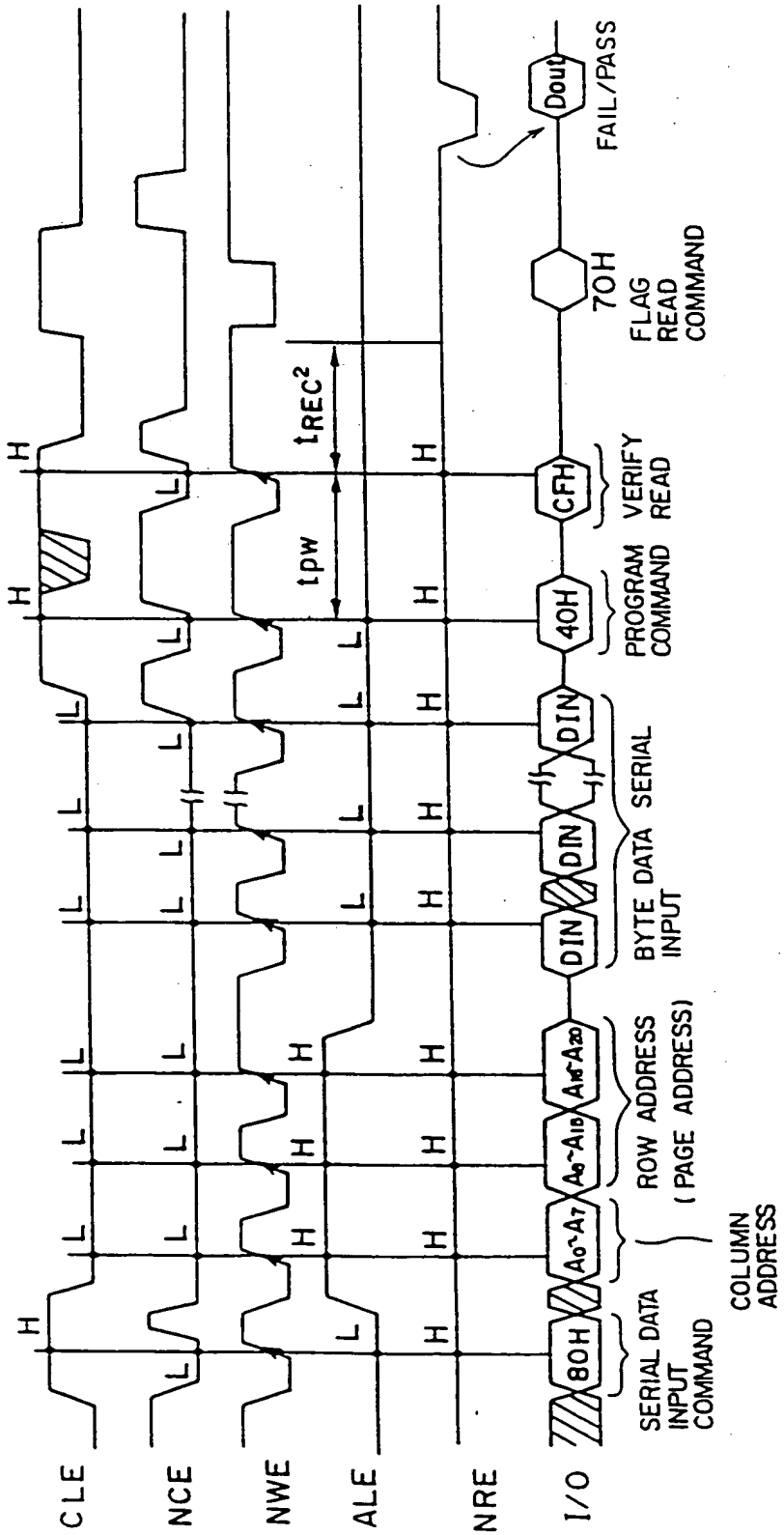

CLE
NCE
NWE
ALE
NRE
I/O
READY/BUSY
H
L
80H
A0~A7
A8~A19
A20
DIN
40H
CFH
tpw
tREC2
Dout
70H
SERIAL DATA INPUT COMMAND
COLUMN ADDRESS
ROW ADDRESS (PAGE ADDRESS)
BYTE DATA SERIAL INPUT
PROGRAM COMMAND
VERIFY READ
FLAG READ COMMAND
FAIL/PASS

FIG. 91

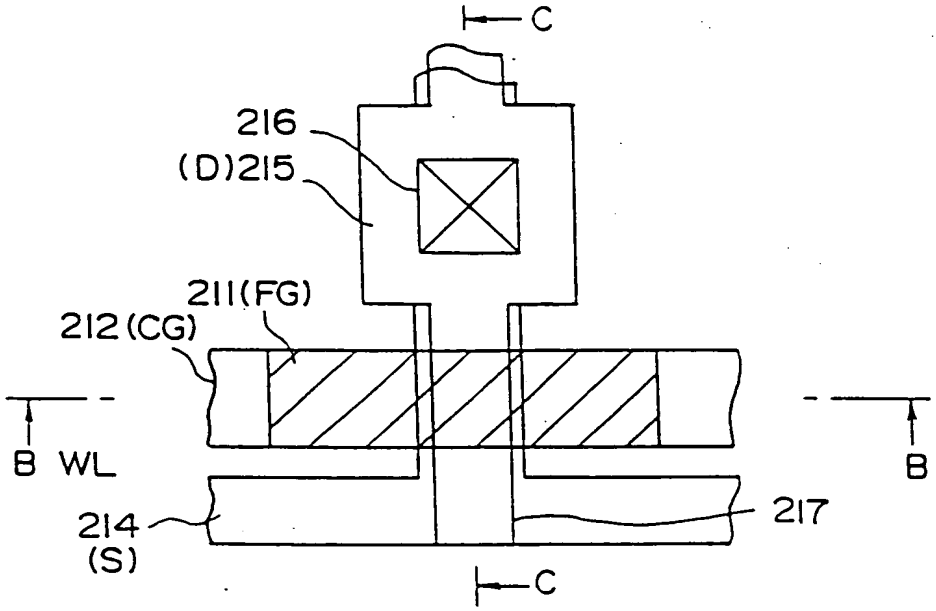


FIG. 92

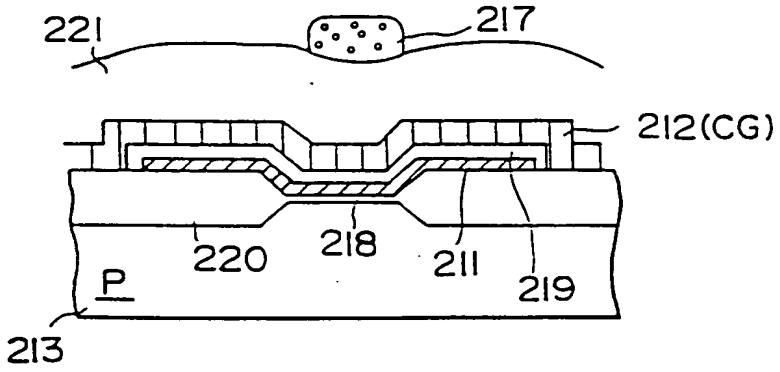


FIG. 93

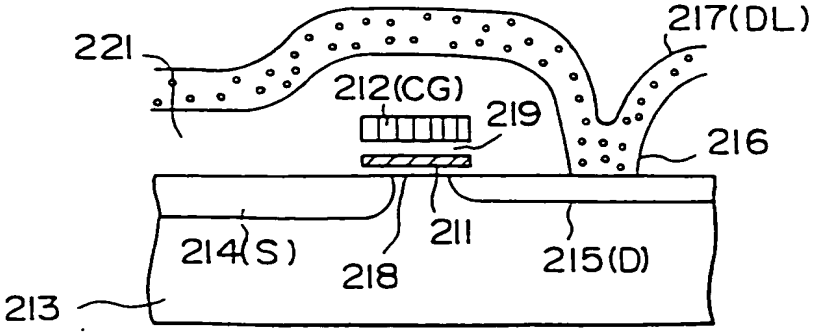


FIG. 94

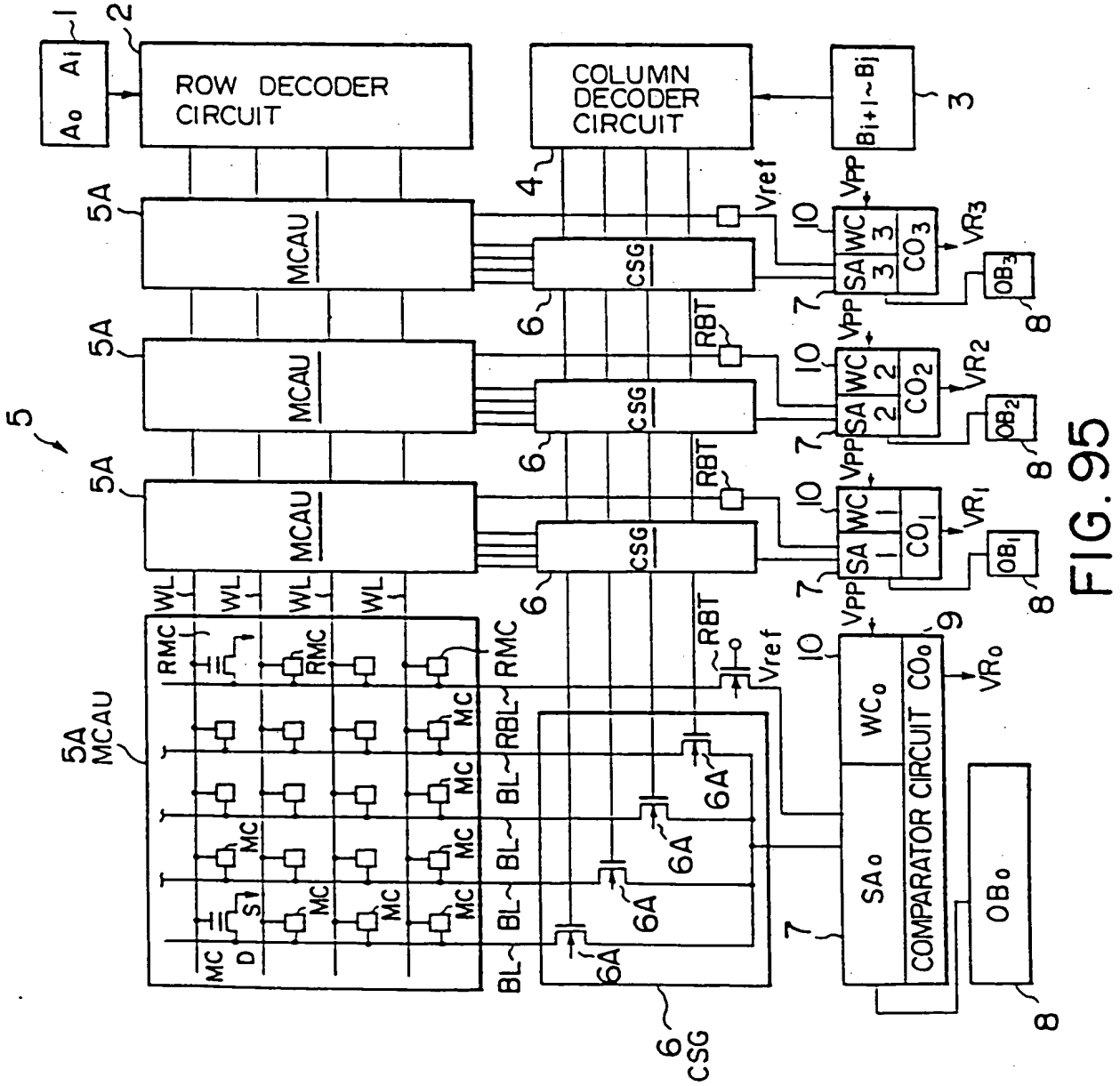

ROW DECODER CIRCUIT
COLUMN DECODER CIRCUIT
MCAU
CSG
WL
RMC
MC
RBL
BL
RBT
Vref
VPP
WC
SA
CO
OB
COMPARATOR CIRCUIT

FIG. 95

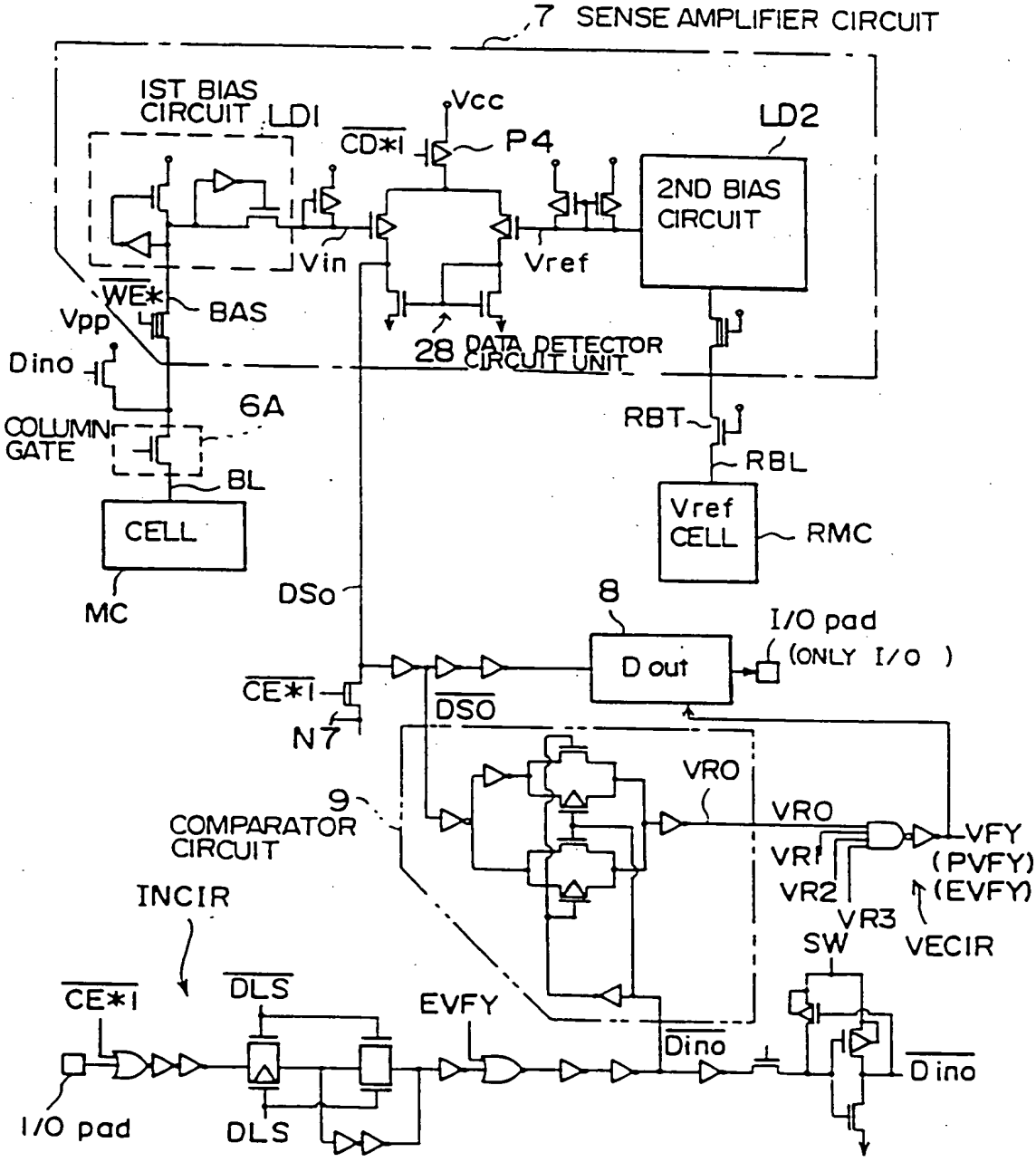

7 SENSE AMPLIFIER CIRCUIT
IST BIAS CIRCUIT
LD1
Vcc
CD*1
P4
LD2
2ND BIAS CIRCUIT
Vin
Vref
WE*
BAS
Vpp
28 DATA DETECTOR CIRCUIT UNIT
Dino
6A
COLUMN GATE
BL
CELL
MC
RBT
RBL
Vref CELL
RMC
DSo
8
D out
I/O pad
(ONLY I/O)
CE*1
N7
DSO
VRO
9
COMPARATOR CIRCUIT
VRO
VFY
(PVFY)
(EVFY)
VR1
VR2
VR3
SW
VECIR
INCIR
CE*1
DLS
EVFY
Dino
Dino
I/O pad
DLS

FIG. 96

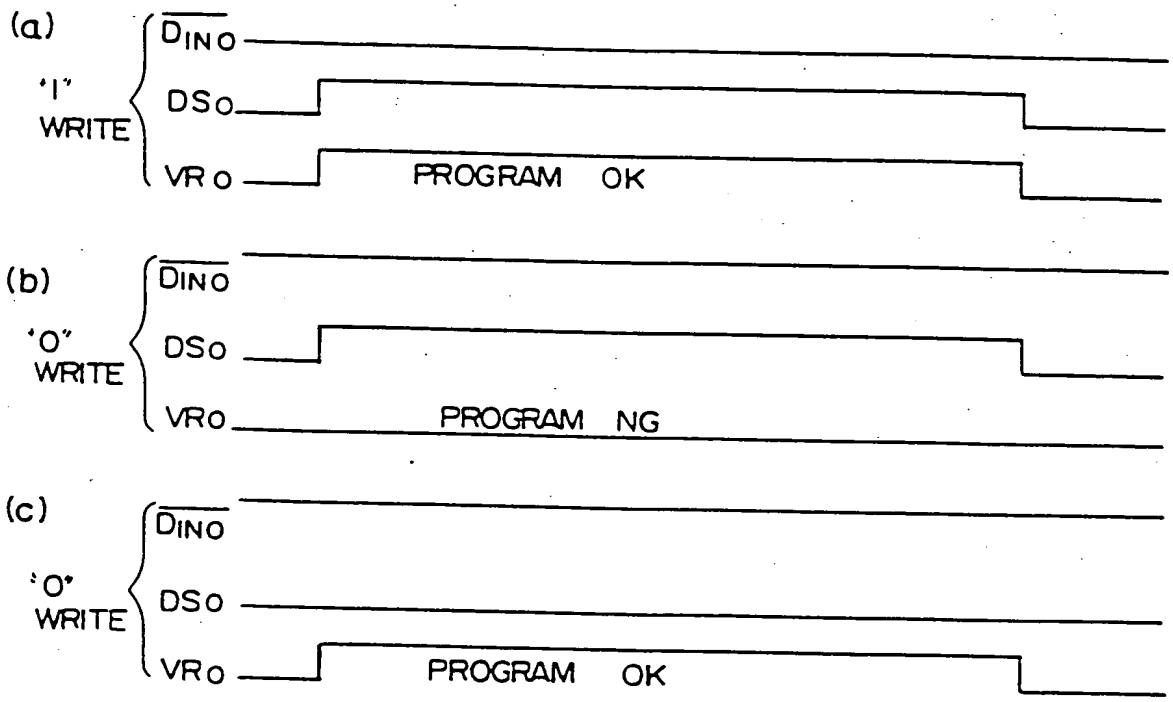

(a)
"1" WRITE
$\overline{D_{IN}}$ o
DSo
VR o
PROGRAM OK
(b)
"0" WRITE
$\overline{D_{IN}}$ o
DSo
VRo
PROGRAM NG
(c)
"0" WRITE
$\overline{D_{IN}}$ o
DSo
VRo
PROGRAM OK

FIG. 97

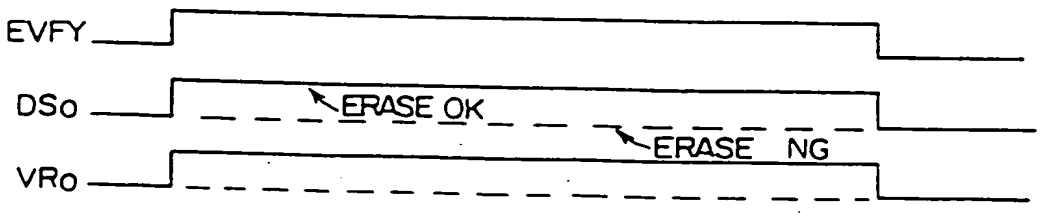

EVFY
DSo
ERASE OK
ERASE NG
VRo

FIG. 98

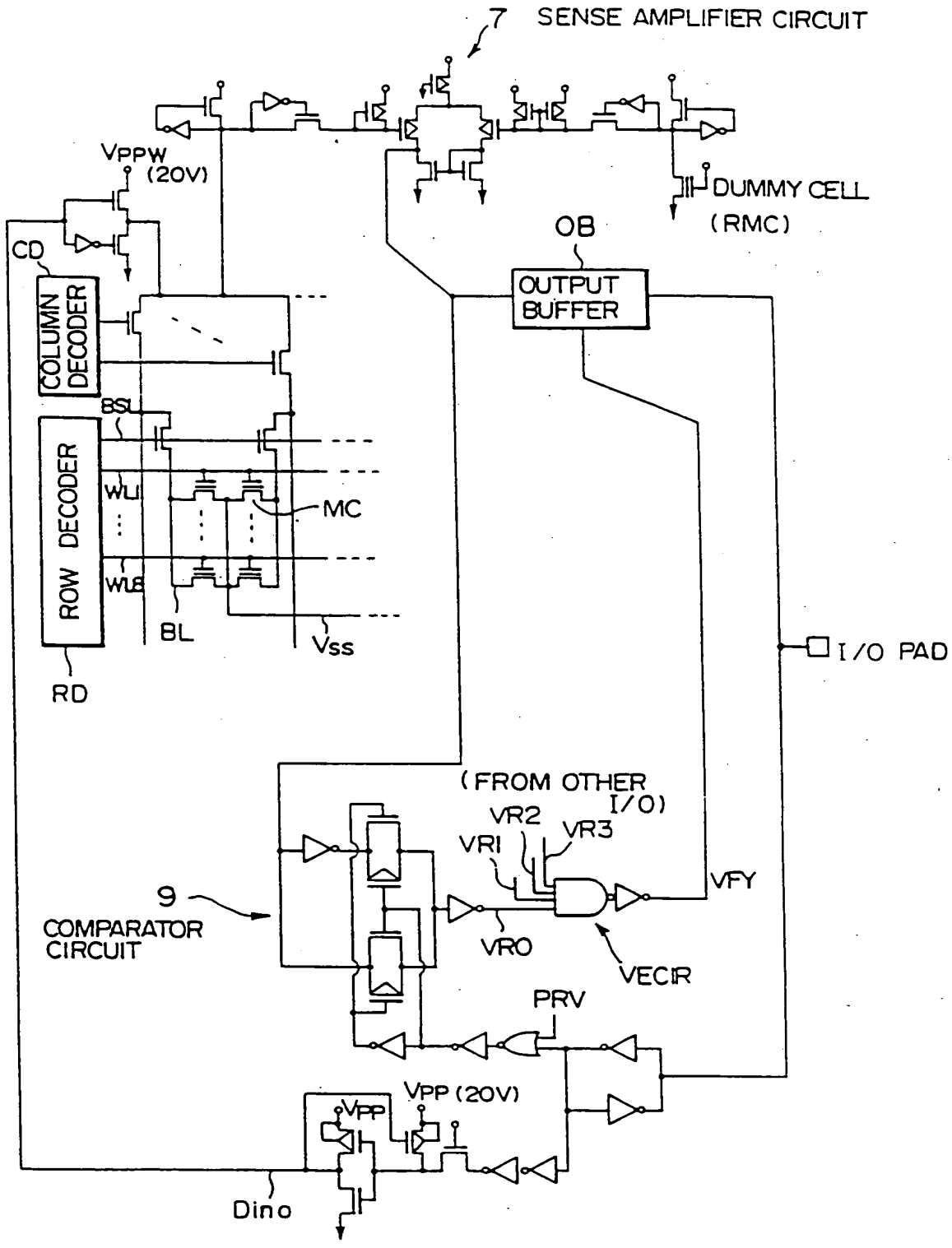

7
SENSE AMPLIFIER CIRCUIT
VPPW (20V)
DUMMY CELL (RMC)
OB
OUTPUT BUFFER
CD
COLUMN DECODER
BSL
ROW DECODER
WLi
WL8
MC
BL
Vss
RD
I/O PAD
(FROM OTHER I/O)
VR2
VR3
VR1
VFY
9
COMPARATOR CIRCUIT
VRO
VECIR
PRV
VPP (20V)
VPP
Dino

FIG. 99

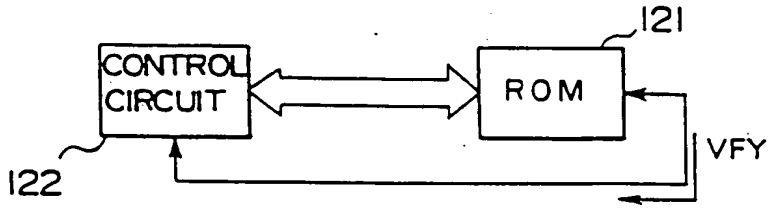


FIG.100

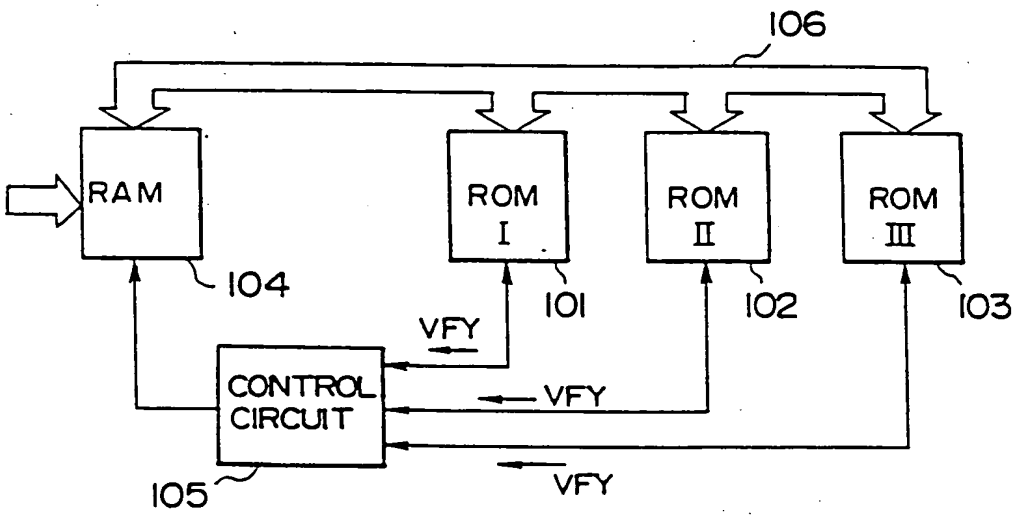


FIG.101

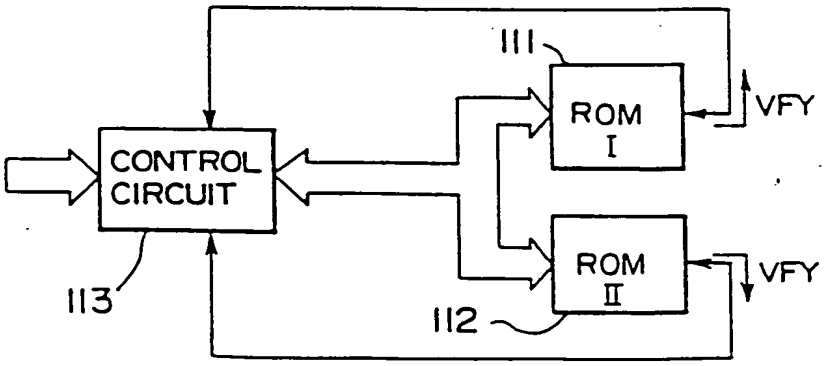


FIG.102